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COMMUNICATIONS SUBSYSTEM FOR THE PETITE AMATEUR NAVY SATELLITE (PANSAT)

by

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Thesis Advisor: Tri T. Ha

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COMMUNICATIONS SUBSYSTEM FOR THE PETITE AMATEUR NAVY SATELLITE (PANSAT)

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ABSTRACT

This thesis describes a prototype design for a binary phase shift keyed (BPSK) direct sequence spread spectrum (DSSS) communications subsystem intended for use in a small lightweight satellite called the Petite Amateur Navy Satellite (PANSAT). The system was designed using parameters that were established from a link analysis. Included as part of this thesis are the link analysis, schematics, and RF board layouts.

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I. INTRODUCTION

The goal of this project is to develop a direct sequence spread spectrum binary phase shift keyed (BPSK) communications subsystem for the Petite Amateur Navy Satellite (PANSAT). Previous work on this topic primarily focused on modulator and demodulator (MODEM) designs that utilized various modulation techniques, such as BPSK, and four frequency shift keying (4-FSK). These MODEMs were designed to operate at 1200 bps, have a pseudo noise sequence length of 127, and have a chip rate (f_{chip}) of 152.4 kHz. With a chip rate of 152.4 kHz, the null to null bandwidth of the transmitted signal was only $2f_{chip} = 304.8\ \text{kHz}$. The link analysis, which determined these and other parameters such as a required transmitter power of 7 watts, was found to be in error. Fortunately, the conservative link analysis that is included as part of this thesis provides communication system performance parameters that far exceed those previously discussed. However, the new parameters called for more bandwidth than was previously understood to be available from the Federal Communications Commission (FCC) and the American Radio Relay League (ARRL). As it turned out, the project only requested 1 MHz of bandwidth, and that is all the ARRL awarded, 1 MHz of bandwidth centered at 437.25 MHz. After a review of all documentation and applicable rules manuals, this too was found to be in error. The rules actually allow space operations anywhere from 435-438 MHz. So to accommodate the wider band signal the center frequency was moved to 436.5 MHz.

Part of the problem was that the communications system was not being looked at, or designed as a system. Previous efforts, in addition to being based on faulty data, ignored the rest of the communications problem by concentrating solely on the MODEM designs. Following the discovery of the errors previously mentioned, it was recognized that the communications problem needed to be approached as a system. So this thesis project was expanded from the design of a MODEM to the design of a complete communications subsystem. The intent was not only to design, but to design, build, and test the complete communications subsystem.

This thesis begins with an explanation and results of the most recent link analysis. Followed by a functional description of the communications subsystem that evolved during the course of this thesis work. The details of this work, such as the schematics and board layouts have been included as appendices. Additional information on pseudo noise sequences, the link analysis, and filter design may also be found in the appendix.

II. LINK ANALYSIS

Before attempting a design of either the transmitter or receiver, a link analysis was performed for both the up-link and down-link. Past experience has shown that even though the link budget equation is very simple, minor errors are easily made. That is why a general link analysis program was written using MATLAB® and included as Appendix B. Most of the equations used in the program came from [Ref. 1:p. 390-396]. Some of these equations are repeated here for clarity. This Matlab® program allows the user to quickly vary the system parameters and plot the results over a wide range of transmitter power. The results are output in both graphical and tabular formats. The tabular format provides, among other things, an estimate of the received carrier power at the base of the antenna. This estimate is then used to compute the power throughout the design.

As one might expect, the receiver will have to process a very weak signal; just how weak is what needed to be determined. The answer was provided by the link analysis program. A main concern was that the noise added by the receiver components might obscure this weak signal. Fortunately, the receiver's noise figure may be controlled though the proper selection of receiver components such as the low noise amplifier (LNA). Once the receivers noise figure is known, the carrier-to-noise-ratio may be computed. Because each amplifier stage amplifies the signal and noise equally, the carrier to noise ratio at the front of the receiver is the same as the carrier to noise ratio at the detector.

$$\left(\frac{C}{N}\right) = \left(\frac{C}{N}\right)_{Rx} = \left(\frac{C}{N}\right)_{det} \tag{2.1}$$

Since this ratio remains constant throughout the receiver, the noise power may be ignored and the signal power used exclusively in power calculations.

Parameters	Values
Gain of Amplifier Stages	G = 22.5, 27, 27, 27 dB
Noise Figures of Amplifier Stages	NF = 2, 1.6, 1.6, 1.6 dB
Earth Station Antenna Gain	G_{Earth} = 12 dB
Satellite Antenna Gain	$G_{Satellite}$ = 0 dB
Antenna Noise Temperature	T_A = 280° Kelvin
Antenna Elevation Angle	E = 5°
Transmitter Carrier Frequency	f_c = 436.5 MHz
Earths Radius	R = 6378.153 km
Altitude of the Satellite	h = 480 km
Speed of light	$c = 2.997925 \times 10^8$ (m/s)
Boltzman's Constant	$k = 1.38 \times 10^{-23}$

Table 2-1: System parameters used in the link analysis.

For the purpose of comparison, the transmitter power was varied from 0.2 watts to 2.0 watts and the resulting effective isotropic radiated power (P_{EIRP}) computed using the following equation.

$$P_{EIRP} = P_t G_t \tag{2.2}$$

Parameters such as P_t and G_t are shown in Table 2-1. Once the P_{EIRP} is known the received carrier power may be computed using equations (2.3) and (2.4). Equation (2.4) is used to determine the amount of loss due to free space.

$$C_{Rx} = (P_{EIRP}) + G_{AR} - L_{FS} \tag{2.3}$$

$$(L_{FS})_{dB} = 20\log\left[\frac{(4\pi d)}{\lambda}\right] \tag{2.4}$$

The noise component of $\left(\frac{C}{N}\right)_{Rx}$ is computed using equations (2.5) through (2.8). These equations are used to compute the system noise temperature. Looking at equation (2.8) it is easy to see why the low noise amplifier (LNA) is the single largest contributor to the receivers noise figure and noise temperature and why its selection in terms of gain and noise figure is so important.

$$N_{Rx} = kT_{syst}B_{IF} \tag{2.5}$$

$$T_{syst} = T_{AR} + T_e \tag{2.6}$$

$$T_e = T_o(F_e - 1) \tag{2.7}$$

$$F_e = F_{LNA} + \frac{F_1}{G_{LNA}} + \frac{F_2}{G_{LNA}G_1} + \ldots + \frac{F_n}{G_{LNA}G_1 \ldots G_n} \tag{2.8}$$

Since this link analysis considers only the worst case, the slant range (d) was only computed for an elevation angle of $E = 5^{\circ}$ using the following equation.

$$d = \sqrt{(R+h)^2 + R^2 - 2R(R+h)\sin\left(\frac{E\pi}{180} + \operatorname{asin}\left(\frac{R}{(R+h)}\right)\cos\left(\frac{E\pi}{180}\right)\right)} \tag{2.9}$$

The results are then converted to dB's, thus reducing the problem to simple addition.

$$(P_{EIRP})_{dBw} = 10\log(P_{EIRP}) \tag{2.10}$$

$$k_{dB} = 10\log(1.38\times10^{-23}) = -228.6_{dB} \tag{2.11}$$

$$B_{dB} = 10\log(B_{IF}) \tag{2.12}$$

$$\left(\frac{C}{N}\right)_{dB} = (P_{EIRP})_{dBw} - (L_{FS})_{dB} + \left(\frac{G_{AR}}{T_{syst}}\right)_{dB} - k_{dB} - B_{dB} \tag{2.13}$$

$$\left(\frac{E_b}{N_o}\right)_{dB} = \left(\frac{C}{N}\right)_{dB} + B_{dB} - R_{dB} \tag{2.14}$$

Now that $\frac{E_b}{N_o}$ is known, the probability of a bit error may be calculated using the error correction function as shown in the following equation.

$$P_b = \frac{1}{2}\left(1 - \operatorname{erf}\left(\sqrt{\frac{E_b}{N_o}}\right)\right) \tag{2.15}$$

A graph of the bit energy-to-noise-ratio as a function of the information bit rate and transmission power is shown below.

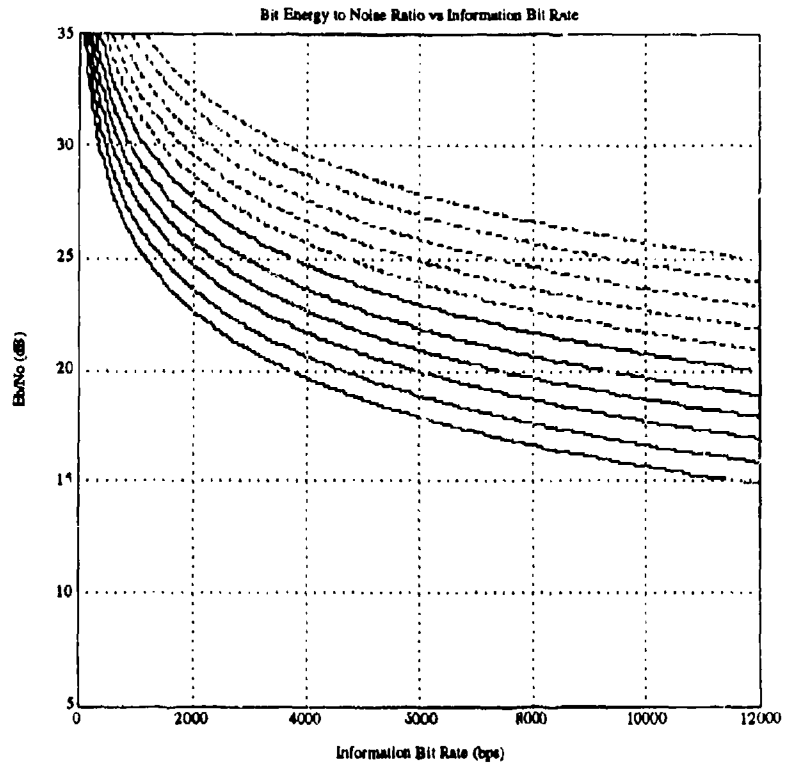


Figure 2-1 Bit energy to noise ratio vs. the information bit rate over a power range from 0.2 to 2.0 watts. The lowest curve is for 0.2 watts.

Graphs showing the probability of error are not included here, because the probability of error is so low, but may be found in Appendix B. Appendix B also contains the MATLAB® program and a set of tabular results for the data in Table 2-1.

III. FUNCTIONAL DESCRIPTION OF THE COMMUNICATIONS SUBSYSTEM

The following discussion is conducted using simplified block diagrams of actual boards designed during the course of this thesis work. Following a brief explanation of the overall system, each board will be discussed individually. If more detail is desired, it may be found in the schematics and layout diagrams included in Appendix D. If the reader requires a review of spread spectrum communications or wishes to see mathematical proofs of concepts applied here, References 5, 7, and 11 are suggested.

Equations used here may be written differently than those found in most text books. In most communications text books a signal is described mathematically as

$$S(t) = \sqrt{2P}\cos(\omega_c t + \theta(t-\tau) - \phi) \tag{3.1}$$

where $\sqrt{2P}$ is the power of the signal, $\theta(t-\tau)$ is the phase modulation with τ representing a phase shift due to the channel, and ϕ is the carrier phase shift due to the channel. Since this thesis is a practical application of communications theory and mathematics, signals will be described in the following way

$$S(t) = P_{dBm}\cos(\omega_c t + \theta(t-\tau) - \phi) \tag{3.2}$$

It seems more practical to write signal equations in this manner, because component catalogs express gain, loss, and power in units of dBs and dBms. Now gains and losses may be accounted for with simple addition and subtraction.

$$S(t) = (P_{dBm} + G_{dB} - L_{IL})\cos(\omega_c t + \theta(t-\tau) - \phi) \tag{3.3}$$

With signal power expressed in this way, the reader may easily apply these equations to the circuits in Appendix D, and use a spectrum analyzer to measure signal levels at critical points in the design. Measurements may be made by simply tuning to the carrier frequency $f_c = \frac{\omega_c}{2\pi}$, adjusting the span to ≥ 2(data rate), and moving the marker to the peak of the signal waveform, which in this case is a SINC^2 function.

A. OVERVIEW OF THE COMMUNICATIONS SUBSYSTEM

Every spread spectrum communications system must perform the same basic functions. The transmitter must spread the data spectrally, up-convert to the carrier frequency, amplify the signal and radiate it from an antenna. Every spread spectrum receiver must down-convert from the carrier frequency, provide doppler compensation if necessary, amplify the received signals, detect the desired signal, track it, de-spread it, and demodulate it. What could be simpler? Well, the devil is in the details.

This communications subsystem affords the user flexibility by providing the ability to:

- Select between redundant transmitters and receivers
- Select a desired transmitter power from a range of power levels
- Evaluate numerous PN phase search strategies, and use the one that provides the quickest acquisition time possible
- Switch between straight BPSK and spread spectrum BPSK
- Compensate for doppler shift using the ground station only
- Develop and test a faster acquisition circuit in the future

Starting with a link analysis this communications subsystem was designed as a system. The design is modular, with each board performing a different and unique function. Circuit design and component selection was based on power levels that were determined from the link analysis and used to calculate the signal power throughout the design. Because of the interdependency on signal power levels between each board, an iterative approach to the design was employed. The design evolved, as the designer became more aware of the practical aspects of circuit design and component selection.

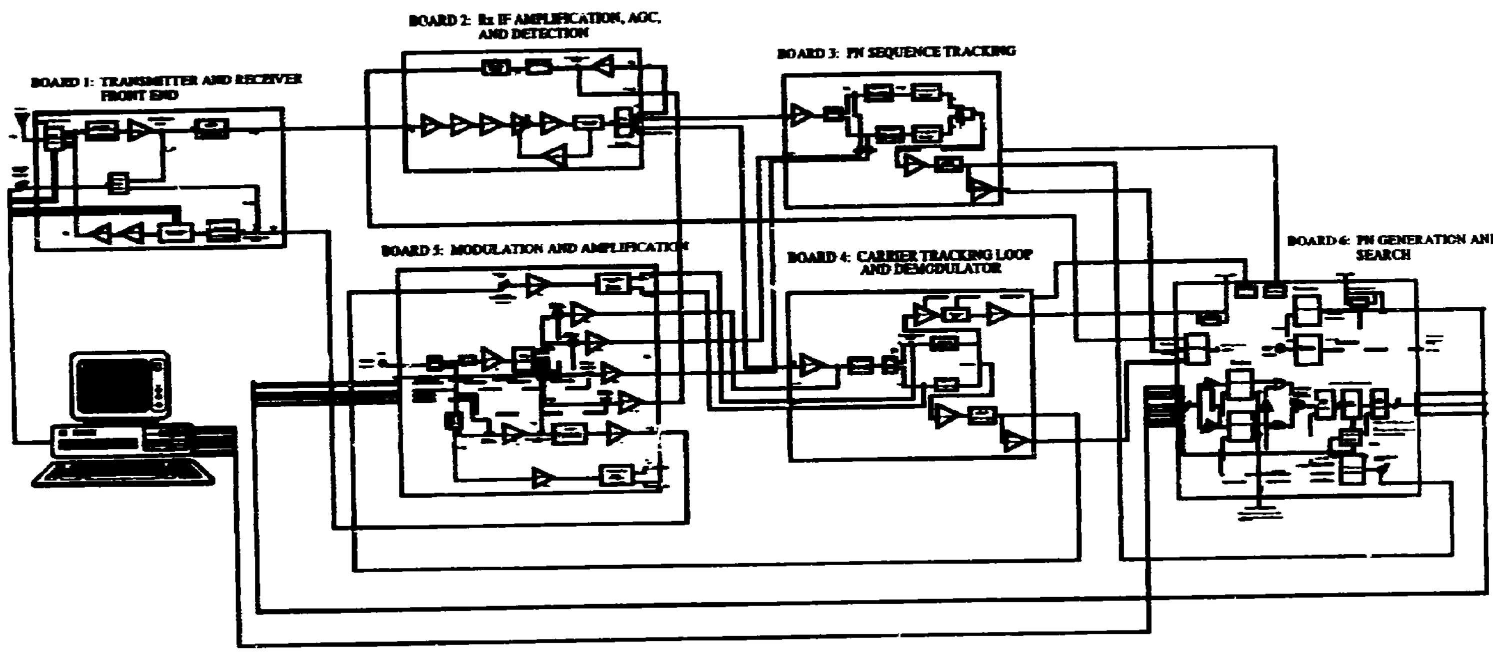


Figure 3-1 Overview of the communications subsystem. The detector, tracker, and demodulator shown here are not unlike those found in references 5, 7, and 11. This high level diagram shows functional connectivity only. It is not intended for use as a connection diagram. The internal functions are shown to more easily correlate these boards with those discussed in the pages that follow.

Figure 3-1 is a functional diagram of the present design, where:

- Board 1: provides up-conversion, down-conversion, and amplification.
- Board 2: provides receiver IF amplification, automatic gain control (AGC), and coarse PN phase detection.
- Board 3: provides fine PN phase alignment and tracking.
- Board 4: de-spreads the signal, locks on to the phase of the suppressed carrier, and demodulates the data.
- Board 5: provides modulation and amplification of PN sequences developed on board 6 and applied to boards 2-4.
- Board 6: provides PN phase generation, search, and control logic, as well as any other digital circuitry used in the design.

Though not yet complete, this design makes significant strides in the right direction. With its flexibility and modularity, the opportunity is there for future designers to continue its evolution or use it as a test bed for new and improved designs.

B. BOARD 1: TRANSMITTER AND RECEIVER FRONT END

Board 1 groups all the components with SMA connectors together. Connections via SMA and 50Ω cable eliminate printed circuit board (PCB) design problems that would likely occur at frequencies above the first IF frequency of 32.1 MHz. Board 1 is designed to serve in either the satellite, using a fixed 404.4 MHz oscillator or in the ground station, using a variable 404.4 MHz oscillator. The variable oscillator's control input will come from a program called the Kansas City Tracker that predicts the orbital track of the satellite. This method of doppler compensation eliminates the need for tunable filters in the satellite and places the burden of doppler compensation solely on the ground station. Another more obvious way to achieve doppler compensation is to simply widen the filter bandwidths. This method was ruled out because the maximum doppler shift is projected to be $\pm$ 10 kHz, while the information bandwidth is $\leq$ 20 kHz null to null, making the noise power bandwidth twice as large as the signal bandwidth.

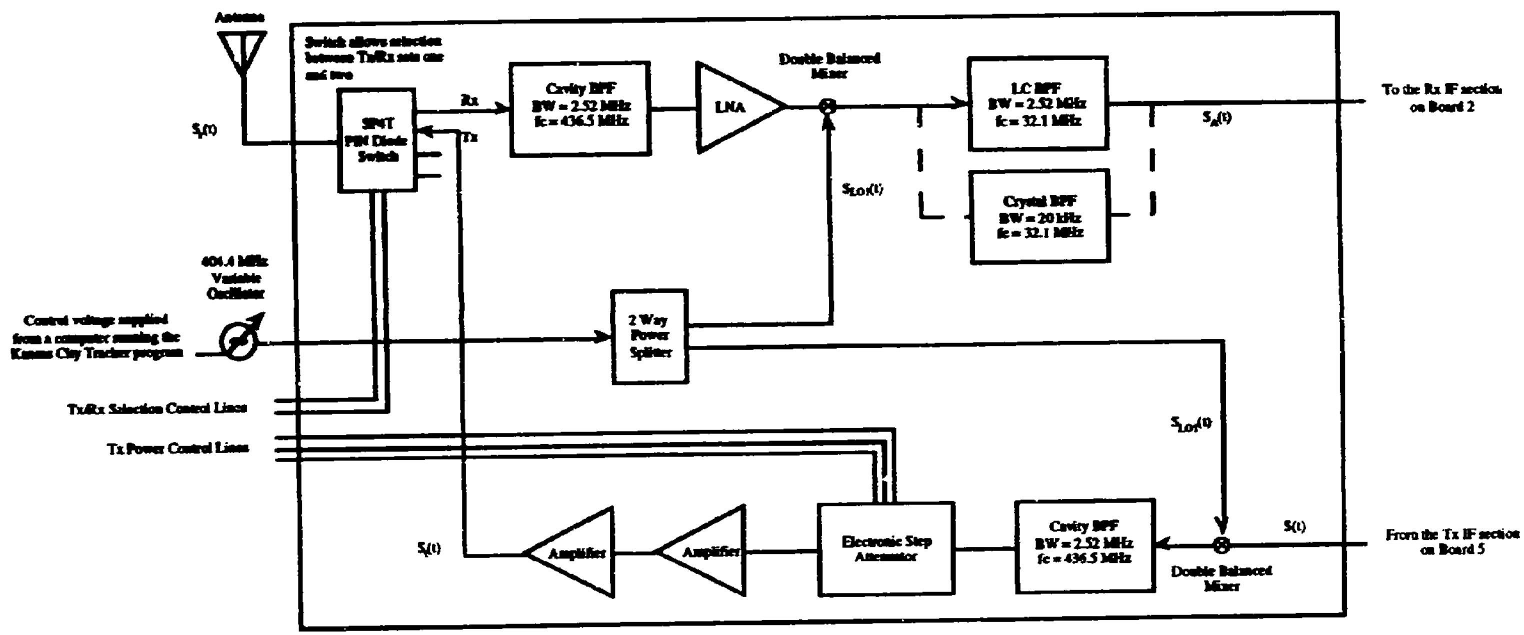


Figure 3-2 Simplified block diagram of Board 1, which performs up-conversion, down-conversion, and amplification. The 404.4 MHz VCXO, shown connected to this board, is used to compensate for doppler in the Tx/Rx of the ground station. Its control voltage is provided by a computer program that predicts the satellites orbital track.

The single pole four throw (SP4T) PIN diode switch allows the user to switch between two receivers and two transmitters, using two TTL control lines. The cavity bandpass filter (BPF) following the SP4T PIN diode switch serves as a preselection filter for the wideband low noise amplifier (LNA). This preselection filter should eliminate strong out of band carriers by reducing the noise power bandwidth. The LNA will provide needed amplification prior to mixing for downconversion to the first IF frequency of 32.1 MHz. The inductor and capacitor (LC) BPF is then used to select the difference frequency from sum and difference frequencies that result from mixing. The output of the LC BPF is then feed to the receiver IF strip on board 2.

The upconverter translates the 32.1 MHz IF frequency from board 5 up to the RF frequency of 436.5 MHz. Here, the BPF following the mixer is used to select the sum of the local oscillator and IF frequencies. A cavity filter is used because of the high Q and high center frequency required by the application. The Q is calculated as:

$$Q = \frac{f_c}{BW} = \frac{436.5\text{MHz}}{2.52\text{MHz}} \cong 173 \qquad (3.4)$$

Unfortunately, the size of these filters is very large when compared to other components. However, they are passive and have SMA connectors, as do all the components on this board, so they may be placed anywhere in the satellite.

Because there is still some uncertainty over the amount of power required to complete the link with an acceptable $\frac{E_b}{N_o}$, an electronic step attenuator was built into the design. Detrimental channel effects such as multipath fading, are the primary concern. The electronic step attenuator will allow the controlling ground station to select the most appropriate transmitter power between 0.2 watts and 2.0 watts. The two amplifiers following the electronic step attenuator are expected to provide amplification up to a maximum of 2 watts. However, since the project is only in the bread board stage a lower power amplifier was used.

The received signal will arrive with a random PN sequence phase and random carrier phase. Each is indicated in the equations that follow, as τ for the PN sequence phase and ϕ for the carrier phase. For simplicity, additive channel noise is neglected.

$$S_r(t) = P_{r\,(dBm)} \cos[\omega_c t + \theta_d(t-\tau) - \phi] \tag{3.5}$$

As mentioned above, LO1 may be either fixed or variable depending on the application. Only the fixed oscillator is considered here.

$$S_{LO1}(t) = (P_{dBm} - 3_{dB} - L_{IL}) \cos(\omega_{LO1} t) \tag{3.6}$$

$$S_{LO1}(t) = P_{7dBm} \cos(\omega_{LO1} t) \tag{3.7}$$

After down-conversion to the first IF frequency, the following is delivered to the receiver IF strip on board 2.

$$S_A(t) = P_{A\,(dBm)} \cos[(\omega_c - \omega_1)t + \theta_d(t-\tau) - \phi] \tag{3.8}$$

$$P_{A\,(dBm)} = P_{r\,(dBm)} - L_{IL1} + G_{LNA} - L_{conv} - L_{IL2} \tag{3.9}$$

$$S_A(t) = P_{A\,(dBm)} [\cos\omega_{IF1} t + \theta_d(t-\tau) - \phi] \tag{3.10}$$

The upconverter for the transmitter occupies the bottom half of the board. Its input comes from board 5.

$$S(t) = P_{F\,(dBm)} \cos(\omega_{IF1} t + \theta_d(t)) \tag{3.11}$$

Naturally, the same local oscillator (LO1) is used for the upconversion to the RF frequency.

$$S_{LO1}(t) = P_{7dBm} \cos(\omega_{LO1} t) \tag{3.12}$$

Following upconversion and amplification, the signal delivered to the antenna is

$$S_t(t) = P_{t\,(dBm)} \cos(\omega_{IF} t + \theta_d(t)) \tag{3.13}$$

$$P_{t\,(dBm)} = P_{F\,(dBm)} - L_{conv} - L_{Attn} + G_{21} + G_{22} \tag{3.14}$$

With only a few minor changes, this design may operate in either spread spectrum BPSK and straight BPSK. The addition of a PIN diode switch and narrowband filter, in parallel with the wideband filter following the mixer in the receive path, is necessary to reduce the noise power delivered to boards 2 and 4. The PIN diode switch would be used to select the correct filter, based on the desired mode of operation. Next, the output from board 6 could be switched high, to lock the bi-phase modulators on board 5 in the zero phase state. The controller would then only look to boards 2 and 4 for an indication of detection and lock. On the transmit side, no change to the filter bandwidths is necessary. Naturally, since the signal is to remain narrowband, the XOR gate on board 6 would be switched out. So, only boards 1 and 6 are affected by this change in the mode of operation.

C. BOARD 2: RECEIVER IF AMPLIFICATION, AGC, AND DETECTION

The receiver IF strip and detection circuits were placed on the same board for convenience because they are both relatively small circuits. However, to allow for testing of a different detection circuit in the future, the two are connected via a 50Ω cable.

The receiver IF strip provides amplification and automatic gain control (AGC) prior to distribution to the detection, tracking, and demodulation circuits. An AGC circuit was built into the design to compensate for anticipated signal fading due to multipath and the satellite's tumbling. A predetection feedback path was used, as a result of information read in [Ref. 4:p. 1624-1628] and the fact that it was easier to build.

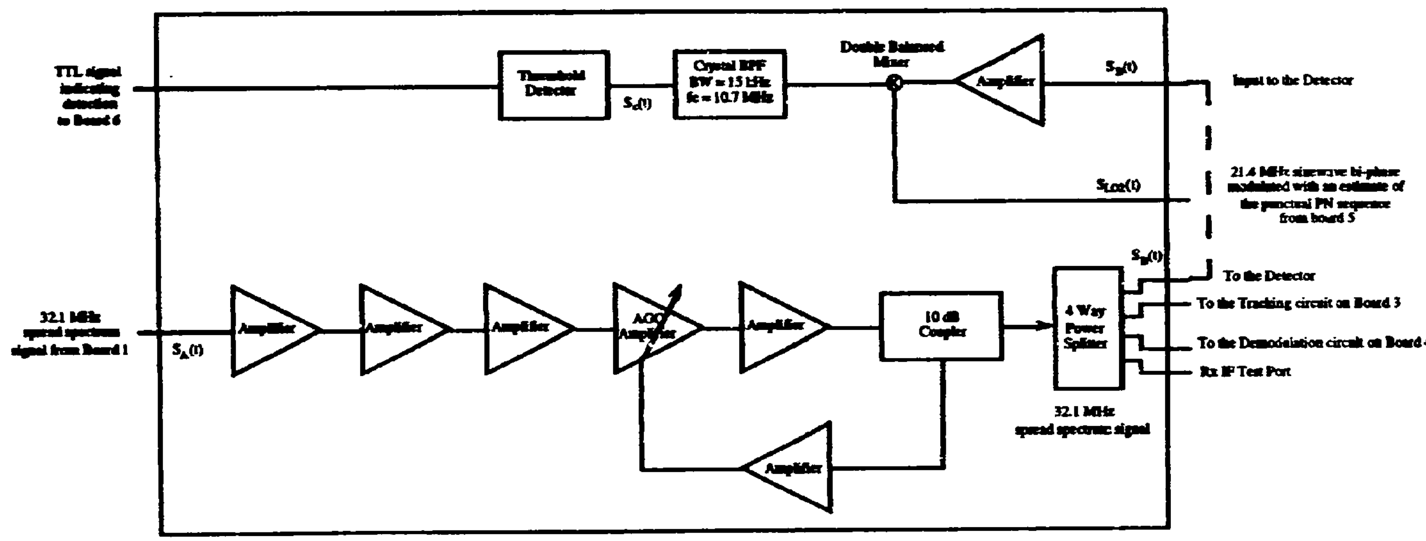


Figure 3-3 Simplified block diagram of Board 2, the receiver IF strip and Detection circuit. The dashed line indicates a loop back connection using 50 Ω cable. This allows for testing of a different detection circuit in the future.

The wideband signal coming into the receiver's IF strip may be expressed as

$$S_A(t) = P_{A(dbm)} \cos[\omega_{IF1}t + \theta_d(t-\tau) - \phi] \tag{3.15}$$

and the amplified signal leaving the IF strip as

$$S_B(t) = P_{B(dBm)} \cos(\omega_{IF1}t + \theta(t-\tau) - \phi) \tag{3.16}$$

where $P_{B(dBm)}$ is a result of the gains and losses seen by the signal along the IF strip.

$$P_{B(dBm)} = P_{A(dBm)} + G_2 + G_3 + G_4 + G_5 + G_{AGC}\Big|_{-14dB}^{22dB} - L_{IL(ALD)} - 6_{dB} - L_{IL} \tag{3.17}$$

The AGC amplifier used in the circuit and expressed in equation 2.3 provides both amplification and attenuation over a range of 36 dB [Ref. 6:p. (14-18)]. Naturally, the amount of gain provided by the AGC amplifier is a function of the voltage output from the analog level detector. This voltage (V_{ALD}) is in millivolts and must be amplified in order to provide a feedback voltage that varies between zero and five volts.

$$G_{AGC} = F(V_{ALD}G_6) \tag{3.18}$$

Once amplified, the signal is distributed to the detection, tracking, and demodulation circuits via a four-way power splitter.

The detection circuit receives its input from the four way power splitter on the same board via a 50Ω cable to allow for the connection and testing of a different detection circuit in the future. This circuit is an implementation of a single dwell detector. The concept is very simple. A search algorithm, implemented using digital components, is used to shift the phase of the locally generated PN sequence. This locally generated PN sequence is then bi-phase modulated onto a carrier from LO2, amplified, and input to the local oscillator port of the mixer

$$S_{LO2}(t) = P_{7dBm} \cos[\omega_{LO2}t + \theta_c(t-\hat{\tau})] \tag{3.19}$$

When the received and locally generated PN sequences come within 1/2 of a chip, the received signal will be de-spread from wideband to narrowband. The narrowband BPSK signal will 'pop-up' in the BPF following the mixer. To limit the amount of noise power bandwidth, the bandwidth of this filter should kept as narrow as possible. Since data is not recovered in the detector, intersymbol interference is not a major concern. In fact, the bandwidth may be as low as one times data rate, to improve performance in a high noise environment [Ref. 5:p. 161]. To achieve a narrow bandwidth at the second IF frequency, a high Q filter was required.

$$Q = \frac{f_c}{BW} = \frac{10.7\text{MHz}}{15\text{kHz}} \cong 713 \tag{3.20}$$

A crystal filter was the only way to achieve a Q this high. Once de-spread and filtered the signal may then be detected. The threshold detector receives its signal from the crystal filter, then provides a TTL signal to board 6, indicating coarse phase alignment.

The autocorrelation of the received and locally generated PN sequences is a stochastic process. Thus the reason the search algorithm must dwell for a period of time, generally the code sequence length, before a decision can be made. If $c(t)$ is a PN code sequence then the autocorrelation of $c(t)$ and a shifted version of itself $c(t-\tau)$ may be expressed as

$$R_c(\tau) = E\langle c(t)c(t-\tau)\rangle = E[c^2] - (E[c])^2 = \sigma^2 - \mu^2 = \text{var} - (\text{mean})^2 \tag{3.21}$$

or

$$R_c(\tau) = \frac{1}{N}\int_{-\frac{N}{2}}^{\frac{N}{2}} \overline{c(t)c(t-\tau)}\,dt \tag{3.22}$$

where the overbar denotes the ensemble average [Ref. 7:p. 351]. The autocorrelation function may be viewed conceptually, with respect to threshold detector, as a magnitude scaler to the signal energy in the bandpass filter.

$$S_c(t) = R_c(\tau)P_{c(dBm)}\cos[(\omega_{IF1} - \omega_{LO2})t + \theta_m(t-\tau) - \phi] \tag{3.23}$$

$$S_c(t) = R_c(\tau)P_{c(dBm)}\cos[\omega_{IF2}t + \theta_m(t-\tau) - \phi] \tag{3.24}$$

$$R_c(\tau) = 1 \text{ when } \tau = \varepsilon N \text{ and } R_c(\tau) = -\frac{1}{N} \text{ when } \tau \neq \varepsilon N \tag{3.25}$$

where ε is an integer. When the received and locally generated PN sequences come to within 1/2 of a chip of perfect alignment, the energy delivered to the threshold detector should be enough to cause a detection ($|R_c(\tau) P_{c\,(dBm)}| >$ threshold). The level of the threshold may be adjusted by using a variable resistor to change the sensitivity.

D. BOARD 3: RECEIVER TRACKING CIRCUIT

The receiver tracking circuit is an implementation of the non-coherent double dither loop (DDL) [Ref. 5:p. 188-189]. This scheme utilizes two channels instead of one. The use of two channels and a subtraction circuit provides the error voltage with a sign (±), thus indicating the direction of phase change required to increase correlation. Dithering the early and late PN sequences between the two channels averages out any DC offset or imbalance inherent in the two channels. The frequency at which they are dithered is determined by the bandwidth of the BPF's in the arms of the tracking circuit [Ref.5:p. 175].

$$\text{Dither frequency} \approx \frac{BW_{BPF}}{4} \tag{3.26}$$

The error voltage that is produced is then amplified, lowpass filtered, and fed back to the VCXO of the PN sequence generator on board 6. A window comparator is used to provide a lock detection signal to board 6.

The wideband signal that is supplied to the tracking circuit board 2 may be expressed as

$$S_B(t) = P_{B\,(dBm)} \cos(\omega_{IF1} t + \theta_d (t-\tau) - \phi) \tag{3.27}$$

This signal is then amplified before splitting to provide a stronger signal to each channel.

$$S_c(t) = (P_{BdBm} + G_8 - 3_{dB} - L_{IL}) \cos[\omega_{IF1} t + \theta_d (t-\tau) - \phi] \tag{3.28}$$

$$S_c(t) = P_{c\,(dBm)} \cos[\omega_{IF1} t + \theta_d (t-\tau) - \phi] \tag{3.29}$$

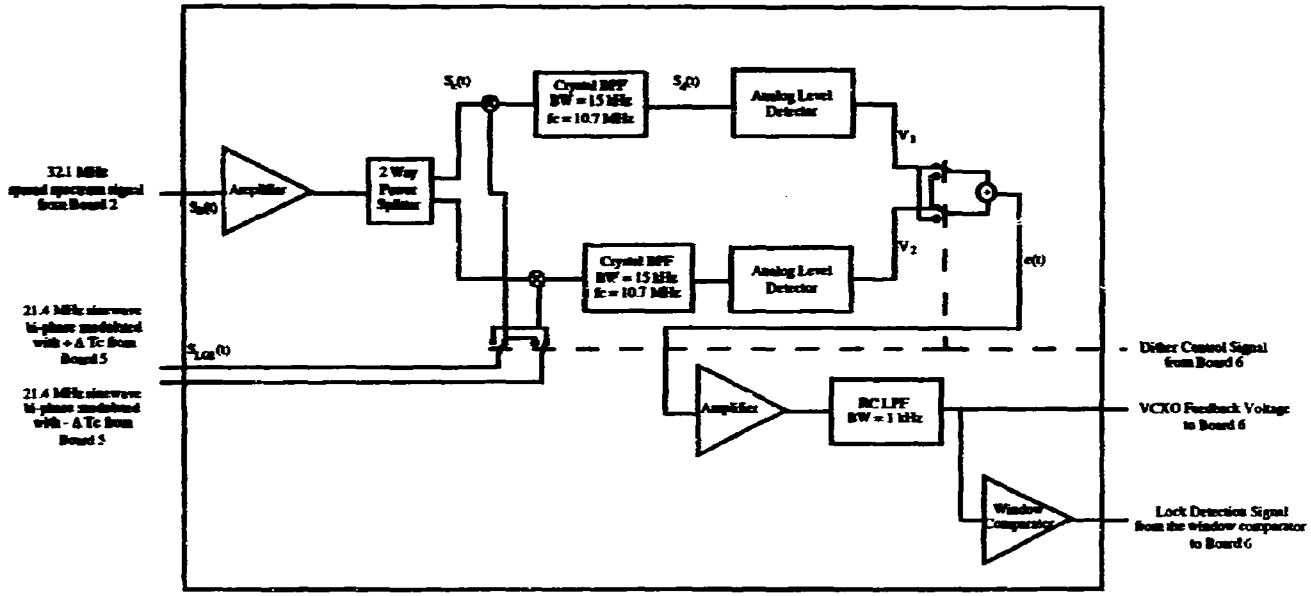


Figure 3-4 Simplified block diagram of Board 3, the receiver tracking circuit. It is an implementation of a non-coherent double dither loop.

The early and late versions of the estimated PN sequence are then used to bi-phase modulate the sinewave produced by LO2. This signal is then amplified to +7dBm and applied to the analog switches used to control the dithering. The other side of these switches is connected to the LO port of the double balanced mixers.

$$S_{LO2}(t) = P_{7dBm}\cos[\omega_{LO2}t + \theta_c(t \pm \Delta T_c - \hat{\tau})] \tag{3.30}$$

The autocorrelation function may be viewed conceptually, with respect to the analog level detector, as a magnitude scaler to the signal energy in the bandpass filter.

$$S_d(t) = (P_{c(dBm)} - L_{conv} - L_{IL\,BPF})R_c(\tau)\cos[(\omega_{IF1} - \omega_{LO2})t + \theta_m(t-\tau) - \phi] \tag{3.31}$$

$$S_d(t) = P_{d(dBm)}R_c(\tau)\cos[\omega_{IF2}t + \theta_m(t-\tau) - \phi] \tag{3.32}$$

The voltage V_1 produced by the analog level detector is obviously a function of the signal power applied to it. Its output varies linearly with the input, as shown in [Ref. 6:p. (5-11)].

$$V_1 = V(|P_{d(dBm)}|) \tag{3.33}$$

As stated before, the error voltage is produced by subtracting the detector outputs of each channel.

$$e(t) = (V_1 - V_2)g(t-nT) \tag{3.34}$$

This error signal will vary in magnitude at the same frequency as the dither signal $g(t-nT)$.

$$\text{Dither frequency} = \frac{1}{T_{dither}} \tag{3.35}$$

Therefore the cutoff frequency of the loop filter should be much less than the dither frequency.

$$BW_{\text{Loop filter}} \ll \frac{1}{T_{\text{dither}}} \tag{3.36}$$

Naturally, this circuit is not used when the communications subsystem is operating in a straight BPSK mode. Everything may still be allowed to function, but neither the feedback voltage nor the loop lock detection are used.

E. BOARD 4: CARRIER TRACKING LOOP AND DEMODULATOR

The demodulating circuit is an implementation of a Costas loop [Ref. 7:p. 145] and [Ref. 1:p. 293]. Its input comes from the four-way splitter on board 2.

$$S_B(t) = P_{B(dBm)} \cos(\omega_{IF1}t + \theta_d(t-\tau) - \phi) \tag{3.37}$$

Assuming acquisition is successful, the locally generated PN sequence is in phase with the received PN sequence. So $\hat{\tau} = \tau$ and $\theta_c(t-\hat{\tau})$ is a punctual version of $\theta_c(t-\tau)$.

$$S_{LO2}(t) = P_{7dBm} \cos(\omega_{LO2}t + \theta_c(t-\tau)) \tag{3.38}$$

Since the received signal is being de-spread with a punctual version of the PN sequence, the autocorrelation function is unity and the signal is maximum.

$$S_c(t) = R_c(\tau) P_{c(dBm)} \cos[(\omega_{IF1} - \omega_{LO2})t + \theta_m(t-\tau) - \phi] \tag{3.39}$$

$$P_{c(dBm)} = P_{B(dBm)} + G_{10} - L_{conv} - 3_{dB} - L_{IL} \tag{3.40}$$

Now that the phase of the PN sequences is locked, the BPSK signal must be demodulated. However, before demodulation can take place, the suppressed carrier must be tracked. A Costas loop is a phase locked loop designed to lock on to suppressed carrier signals. Like the tracking circuit, this scheme also utilizes two channels. But, the signals in these channels are in quadrature.

$$S_{IF2a}(t) = P_{7dBm} \cos(\omega_{IF2}t - \hat{\phi}) \tag{3.41}$$

$$S_{IF2b}(t) = P_{7dBm} \cos\left(\omega_{IF2}t + \frac{\pi}{2} - \hat{\phi}\right) \tag{3.42}$$

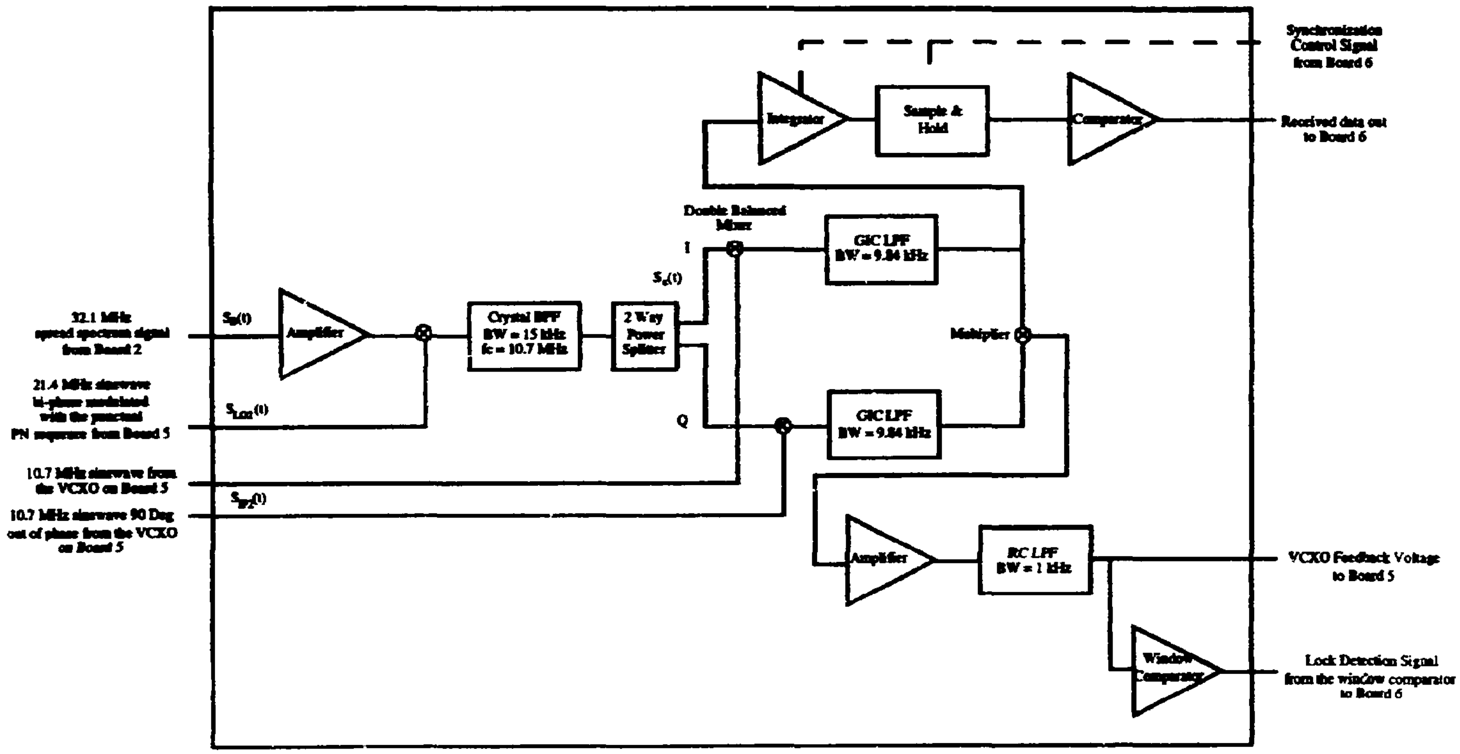


Figure 3-5 Simplified block diagram of Board 4, the receiver demodulating circuit. It is an implementation of a Costas loop.

Since they are in quadrature, the multiplication of the two channels yields their phase difference. This phase difference is expressed as an error voltage that is amplified, filtered and fed back to a 10.7 MHz VCXO on board 6.

$$S_I(t) = (P_{cdBm} - L_{conv} + G_{GIC}) \cos[(\omega_{IF2} - \omega_{IF2})t + \theta_m(t-\tau) - \hat{\phi}] \quad (3.43)$$

$$S_Q(t) = (P_{cdBm} - L_{conv} + G_{GIC}) \cos\left[(\omega_{IF2} - \omega_{IF2})t + \frac{\pi}{2} + \theta_m(t-\tau) - \hat{\phi}\right] \quad (3.44)$$

Now that the correct phase has been determined for both the locally produced PN sequence and 10.7 MHz oscillator, the BPSK signal may now be demodulated. Coherent demodulation is accomplished with an integrate and dump circuit. The integrate and dump is implemented with an active integrator followed by a sample & hold circuit. The result is a NRZ signal that may be converted to digital with a comparator. The timing signal needed to control the integrate and dump is be derived from the PN sequence clock. This is possible because each data bit is an integer multiple of a PN sequence chip. The output of the sample & h' ·ircuit may then be written as

$$m(t-\tau) = V_d e^{j\hat{\phi}} e^{j\theta_m(t-\tau)} = \pm 1 \quad (3.45)$$

where $\hat{\phi} = \phi$ and $e^{j\hat{\phi}} = 1$. The NRZ signal $m(t-\tau)$ is then input into a comparator and converted to a binary message string $m(t-\tau) = (0,1)$.

F. BOARD 5: MODULATION AND AMPLIFICATION

To reduced the number of components on boards 3 and 4 (the tracking and demodulation circuits), the modulation and amplification circuits of these boards were placed on a new board named board 5. This board later became the modulation and amplification board for both the transmitter and receiver.

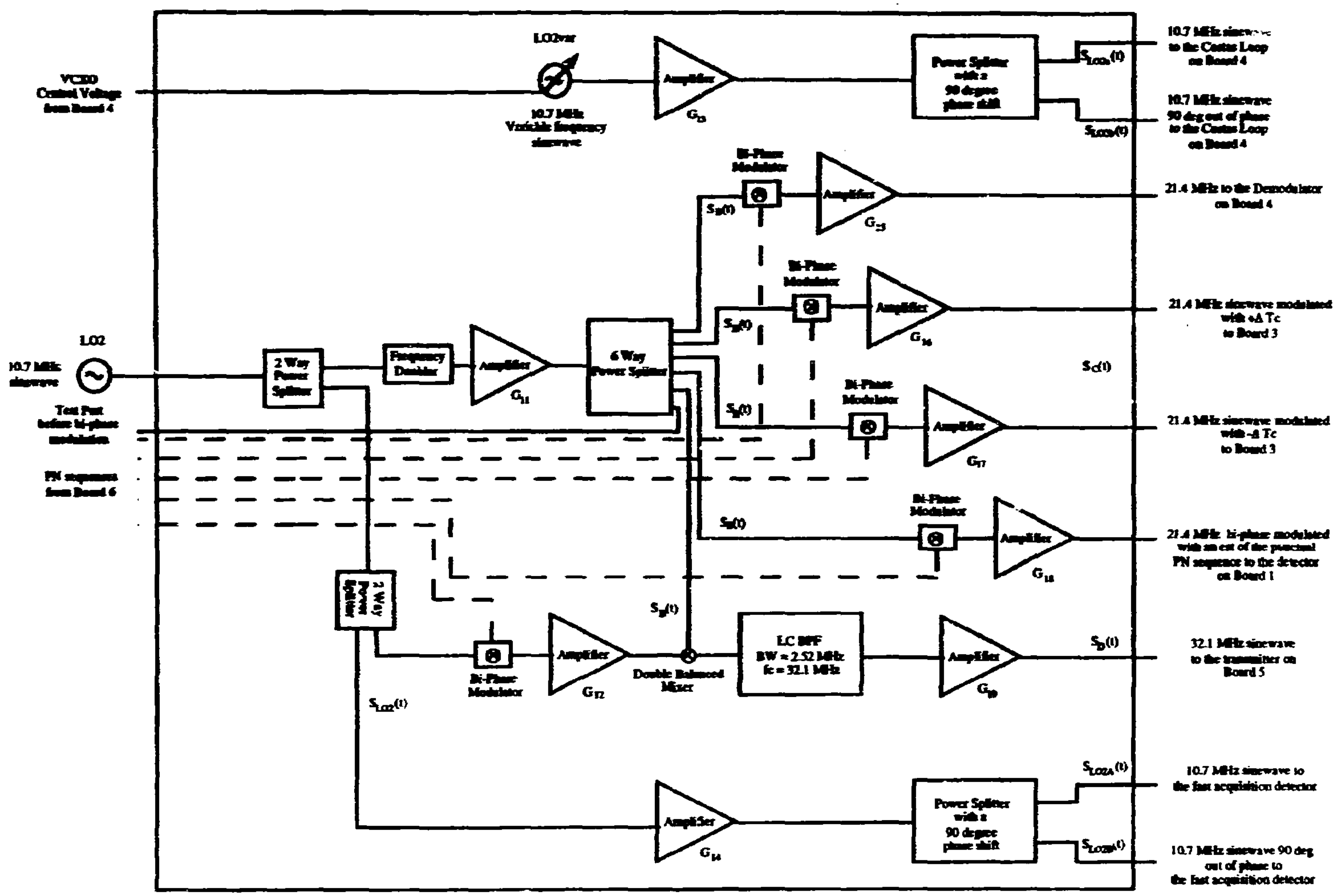


Figure 3-6 Modulation and amplification circuits for both the Tx/Rx.

The circuit that produces S_{LO2A} and S_{LO2B} will allow testing of a faster acquisition circuit in the future.

$$S_{LO2}(t) = (P_{7dBm} - 3_{dB} - L_{IL} - 3_{dB} - L_{IL}) \cos(\omega_{LO2} t) \tag{3.46}$$

$$S_{LO2A}(t) = (P_{7dBm} - 3_{dB} - L_{IL} - 3_{dB} - L_{IL} + G_{14} - 3_{dB} - L_{IL}) \cos(\omega_{LO2} t) \tag{3.47}$$

$$S_{LO2B}(t) = (P_{7dBm} - 3_{dB} - L_{IL} - 3_{dB} - L_{IL} + G_{14} - 3_{dB} - L_{IL}) \cos\left(\omega_{LO2} t + \frac{\pi}{2}\right) \tag{3.48}$$

Modulation and amplification of the data to be transmitted, is provided by the circuit which yields $S_D(t)$.

$$S_A(t) = (P_{7dBm} - 3_{dB} - L_{IL} - 3_{dB} - L_{IL} + G_{12}) \cos(\omega_{LO2} t + \theta_d(t - \hat{\tau})) \tag{3.49}$$

$$S_A(t) = P_{A(dBm)} \cos(\omega_{LO2} t + \theta_d(t - \hat{\tau})) \tag{3.50}$$

$$S_D(t) = (P_{A(dBm)} - L_{conv} - L_{IL} + G_{19}) \cos[(\omega_{LO2} + \omega_{LO3}) t + \theta_d(t)] \tag{3.51}$$

Circuit at the top of the board that produces S_{LO2a} and S_{LO2b}, provides an in phase and quadrature 10.7 MHz sinewave to the Costas loop on board 4.

$$S_{LO2a}(t) = (P_{7dBm} + G_{13} - 3_{dB} - L_{IL}) \cos(\omega_{LO2} t - \hat{\phi})$$

$$S_{LO2b}(t) = (P_{7dBm} + G_{13} - 3_{dB} - L_{IL}) \cos\left(\omega_{LO2} t + \frac{\pi}{2} - \hat{\phi}\right) \tag{3.52}$$

The circuits in the middle of the board perform basically the same function, bi-phase modulation of a PN sequence onto a 21.4 MHz carrier (LO3), after some amplification and power splitting.

$$S_B(t) = (P_{LO2} - 3_{dB} - L_{IL} - L_{conv} + G_{11} - 7.8_{dB} - L_{IL}) \cos(2\omega_{LO2} t) \tag{3.53}$$

$$S_B(t) = P_{B(dBm)} \cos(\omega_{LO3} t) \tag{3.54}$$

$$S_C(t) = (P_{B(dBm)} - L_{IL} + G_{15-18}) \cos(\omega_{LO3} t + \theta_d(t - \hat{\tau})) \tag{3.55}$$

$$S_C(t) = P_{C(dBm)} \cos(\omega_{LO3} t + \theta_d(t - \hat{\tau})) \tag{3.56}$$

G. BOARD 6: PN GENERATOR AND PHASE SEARCH

Due to the lack of time, the design of board 6 is incomplete. The intention was to place all the digital components on one board, thus reducing the number of boards with digital ground. Digital circuits carry signals that have fast rise times and large voltages, especially when compared to the weak analog signals of the RF receiver circuits. The concern is that a noisy digital ground may interfere with the relatively weak analog signals.

1. Transmitter Section

Immediately after the message enters the board it is differentially encoded. This is done to compensate for phase inversion that may occur during the detection process. Naturally, the received message stream will have to be differentially decoded following demodulation in the receiver. The rest of the transmitter circuitry is relatively simple. Once the fixed PN sequence is produced it is exclusively OR'd with the differentially encoded message, and the resulting signal is delivered to board 5 for modulation and transmission. The frequency synthesizer produces timing signals for synchronization of the sending unit.

2. Receiver PN Synchronization Section

Most of the search strategies read about in References 2 and 5 conduct their search for the proper PN phase using discrete shifts of the locally produced PN sequence. Searches such as the one shown in Figure 3-8 may be easily programed, and handled by a microprocessor. However, concerns over power consumption, and allocation of the on-board processors resources lead to an implementation that would require little or no processor interaction. This part of the design is original, and seeks to implement the various search strategies using discrete digital components. A computer is used during the evaluation phase, in order to make it easier to evaluate different search strategies. Once evaluated, the search strategy that provides the quickest access time could be implemented using a state machine to provide the parallel input to the PN sequence generators. If the state machine is too hard to design, then the satellites on board microprocessor should be

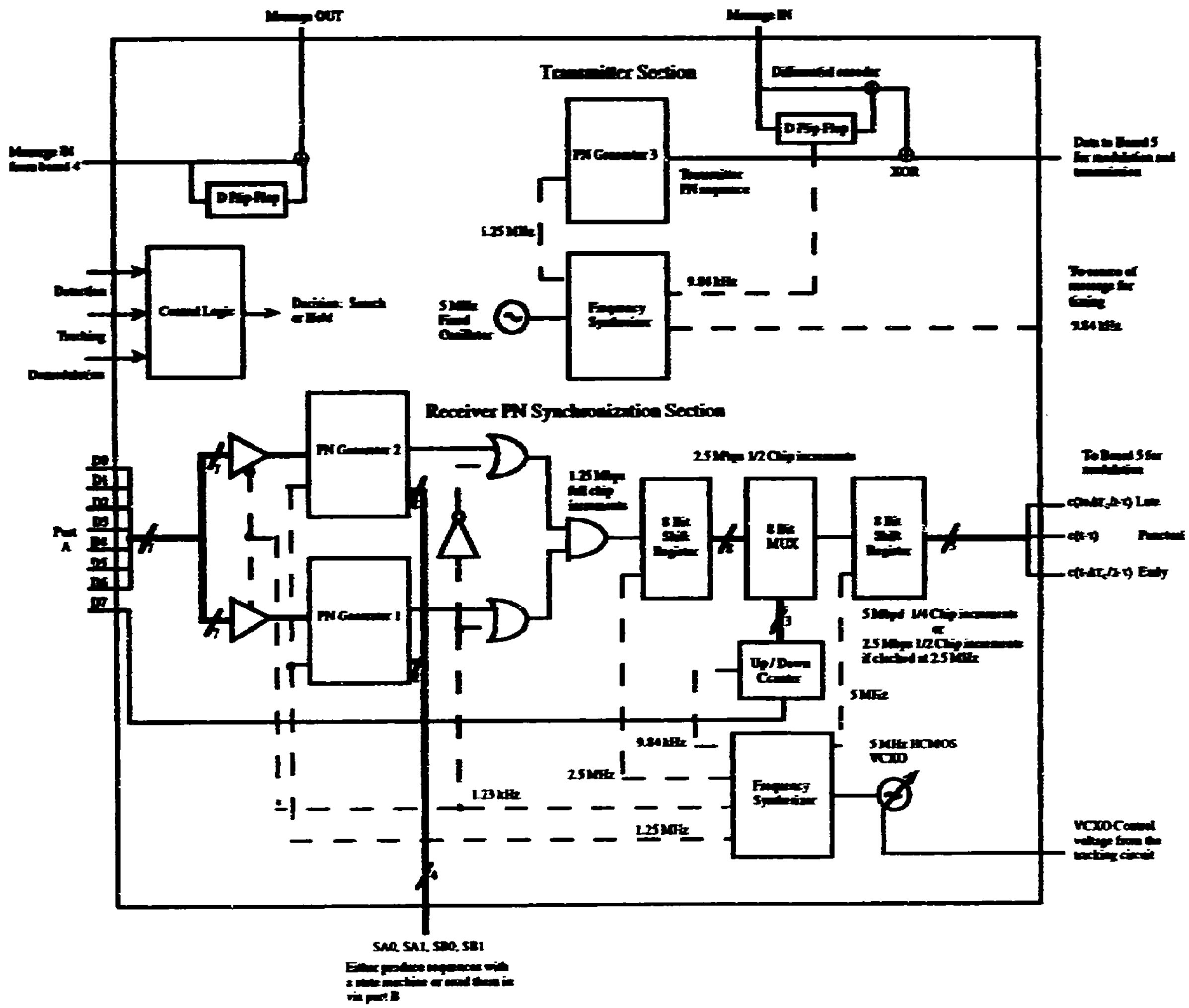


Figure 3-7 Simplified block diagram of Board 6 which provides PN sequence generation, synchronization, and controlling circuitry.

able to provide a seed sequence every 813μs without taxing the microprocessors ability to provide other services. The search strategy shown in Figure 3-8 may be considered a hybrid of those shown and discussed in [Ref. 9:p. 543]. This strategy might be called a broken expanding window, since it is combination of the two.

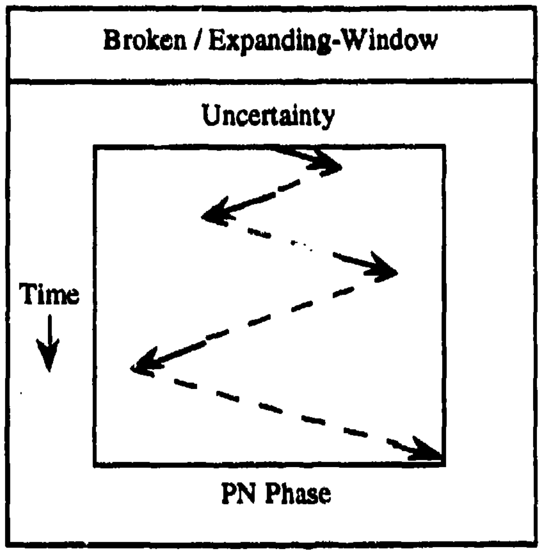


Figure 3-8 Proposed search strategy. A logical extension of the strategies shown in [Ref. 9:p. 543].

The goal is to produce an acquisition system that provides the shortest acquisition time possible. One way to do this is to devise a search strategy that quickly finds the correct phase. Another method is to design a fast detection circuit, such as the one discussed in [Ref. 10:p. 551]. Both were to be tried, unfortunately time ran out. So the faster detection circuit was not attempted. The search strategy shown in the figure above, is a logical extension of the strategies shown in [Ref. 10:p. 543]. This strategy takes advantage of the probability that the correct phase is close to where the search is begun, and minimizes search time by eliminating redundancy during the search.

Two PN sequence generators will be used, one on line and other off line. While the on line PN generator is running, the off line PN generator will load 7 bits of the 127 bits in the sequence. When this generator is placed on line, its sequence will begin with the 7 bits that were loaded. A phase change is introduced by shifting the 7 bits, and a search strategy implemented by programing both the 7 bits and the direction of the up/down counter.

The buffers at the input control which PN generators will load. While the select lines (SA0, SA1, SB0, SB1) control whether the shift registers load, hold, or run. The OR gates to the right of the PN generators are used to control which PN sequence generator is connected to the 8 bit shift register. The up/down counter is then used in conjunction with the 8 bit MUX to choose which line out of the 8 bit shift register is used. The shift register is clocked at twice the rate of the generated sequence, this effectively samples the sequence at twice the frequency. Allowing a search to be conducted in half chip steps. The 8 bit shift register to the right of the MUX may be clocked at either the same frequency as the first shift register or twice the frequency of the first shift register. If clocked at the same frequency, the early and late sequences will be $\pm\frac{T_c}{2}$ from punctual, and if clocked at twice the frequency, they will be $\pm\frac{T_c}{4}$ from the generated sequence. While in search, the VCXO will be fixed at its fundamental frequency. Once detection has been made and tracking has begun, the VCXO is controlled with the feedback from the tracking loop. While tracking, the 7 bit string available on Port A should remain there in case the circuit loses lock and the search must resume. If it does loose lock, odds are that the phase is close to where it was when circuit lost lock. The proposed search strategy is commenced with a parallel loading a 7 bit seed sequence into the shift register. The 8th bit is then used to control the direction of the up/down counter. Looking back at the previous figure, you can see that after one load, the counter may count up, and after another load the counter may count down. With this ability, many different search strategies may be tried.

IV. CONCLUSION

A prototype design of the complete communications subsystem was achieved during the course of this thesis work. This design uses a blend of analog and digital circuits to search and acquire the correct pseudo-noise sequence phase. The project is currently in the bread board phase of its design. Critical areas of the design have been tested using a crude but simple RF bread board technique. Further RF bread boarding is currently under way using boards that have been layed-out and fabricated using a CAD/CAM system. This process, though very time consuming, is cleaner and should provide excellent results. Unfortunately, a complete design of all the digital circuits was not accomplished. However, enough progress was made to start bread boarding and testing the computer interface and search circuitry required for system testing.

A great deal has been learned and accomplished over the course of this design. However, a robust doppler compensation method and circuit remains elusive. The current design utilizes an orbital track prediction program, controlling a VCXO, to provide doppler compensation. This reliance on a prediction program should work, but is an admitted weakness in the design. Additional efforts to provide a more robust solution should be made.

APPENDIX A: PSEUDO NOISE SEQUENCES AND THEIR PROPERTIES

Before going into a theoretical overview of a BPSK spread spectrum communications system, some fundamentals should be covered first. Most of the material on PN sequences was extracted from [Ref. 2:p. 1715-1718], with some re-wording for clarity.

A. Pseudo Noise Sequences

Pseudo noise sequences are also called maximal length sequences, or m-sequences. These sequences, which have a length $N = 2^m - 1$, have properties that are very advantageous to spread spectrum communications, such as their periodic autocorrelation property:

$$R_c(0) = 1 \qquad R_c(\tau) = -\frac{1}{N}, \qquad \text{for } 1 \le \tau \le N-1 \tag{A.1}$$

Maximal length sequences are generated from primitive polynomials and may be constructed using a feedback shift register circuit. Primitive polynomials of degree 'm' are expressed in the following form

$$h(x) = h_m x^m + h_{m-1} x^{m-1} + \ldots + h_2 x^2 + h_1 x^1 + h_0 \tag{A.2}$$

If h(x) is primitive, it can not be factored into a product of two or more polynomials of lower degree. When factored down to its lowest form $h_m = 1$ and $h_0 = 1$. Equation A.2 will then reduce to

$$h(x) = x^m + h_{m-1} x^{m-1} + \ldots + h_2 x^2 + h_1 x^1 + 1 \tag{A.3}$$

where 'm' is the span of the sequence and the number of D-flip flops used to construct the sequence.

The following example is for an m-sequence of length seven. Therefore the length of the generated sequence will be $N = 2^7 - 1 = 127$. The all zeros state is not a valid state.

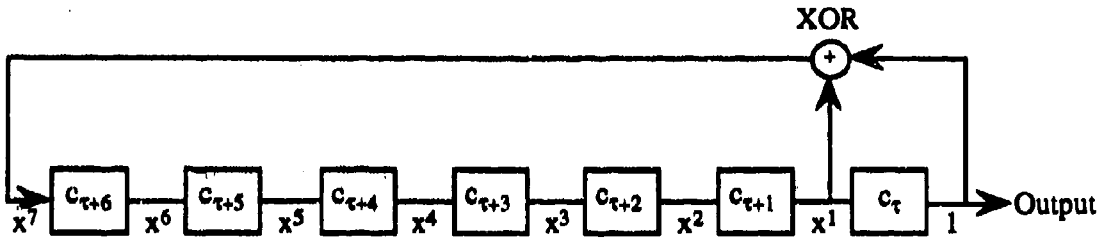


Figure A-1 Feedback shift register for a primitive polynomial of degree $m = 7$, and length $N = 2^7 - 1 = 127$. The generator polynomial is $x^7 + x + 1$.

This feedback shift register generates an infinite sequence $c_0 c_1 c_2 \ldots c_\tau \ldots$ that satisfies the recurrence

$$c_{\tau+7} = c_{\tau+1} + c_\tau, \quad \tau = 0, 1, \ldots \tag{A.4}$$

In the figure above, the output is taken from the last D-flip flop in the chain. However, the same sequence may be seen, with a shift in phase, on the output of any other flip flop in the chain.

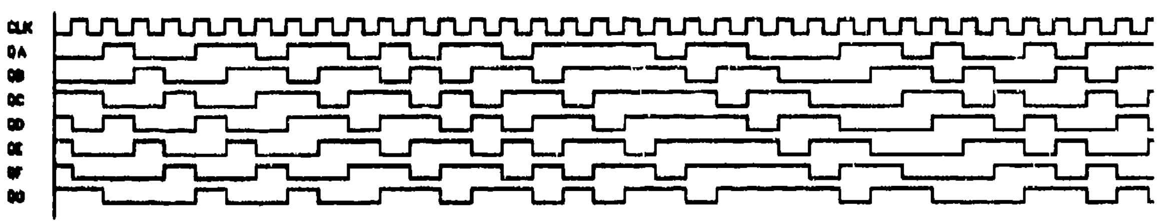


Figure A-2 Timing diagram for the circuit in figure 2-3 which was used to implement the primitive polynomial $x^7 + x + 1$. This timing diagram also demonstrates the shift property.

One way to implement this feedback shift register is as follows:

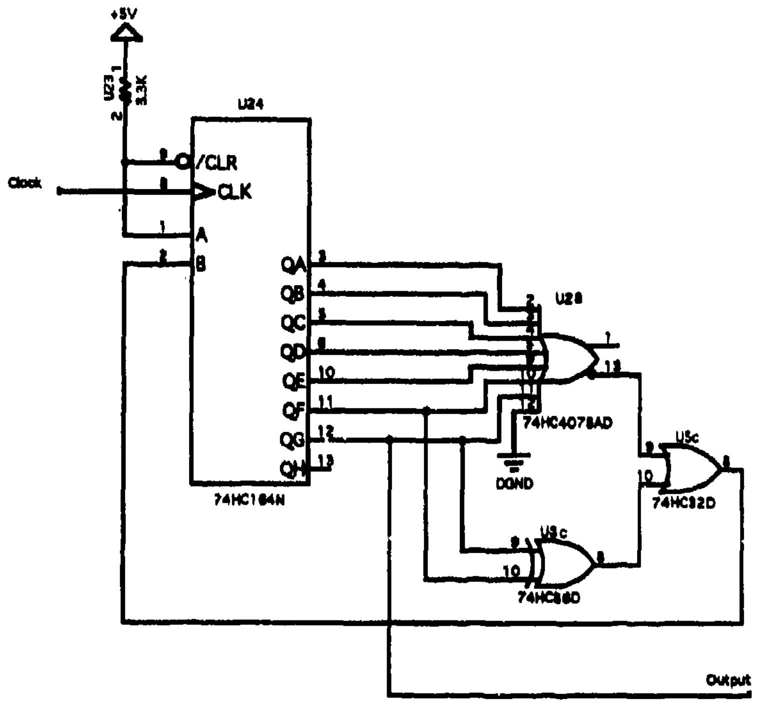


Figure A-3 Circuit implemention of the primitive polynomial $x^7 + x + 1$.

B. Properties of Maximal Length Sequences

The following properties characterize PN sequences and provide the reader with the background necessary to properly apply them to an application such as spread spectrum communications.

1. **The Shift Property:** For a PN sequence of length $2^m - 1$, there are $2^m - 2$ possible shifts of the original. Each cyclic shift produces another PN sequence. The original and the $2^m - 2$ cyclic shifts produces a set δ_m whose size is $(2^m - 1) \times (2^m - 1)$.

2. **The Recurrence Property:** Any PN sequence $c \in \delta_m$ satisfies the recurrence

$$c_{\tau+m} = h_{m-1}c_{\tau+m-1} + h_{m-2}c_{\tau+m-2} + \ldots + h_1 c_{\tau+1} + c_\tau \qquad \text{for } \tau = 0, 1, \ldots \qquad \text{(A.5)}$$

There are 'm' linearly independent solutions to Equation A.5, so there are 'm' linearly independent sequences in the set δ_m.

3. **The Window Property:** If a window of width 'm' is slid along a PN sequence in the set δ_m, each of the $2^m - 1$ nonzero binary m-tuples is seen exactly once. This property follows from the fact that the PN sequence was generated from a primitive polynomial.

4. **The Half 0's and Half 1's Property:** A PN sequence contains 2^{m-1} ones and $2^{m-1} - 1$ zeros. Therefore there will always be one more one than there are zeros in a PN sequence.

5. **The Addition Property:** The sum of two sequences forms another sequence in the set δ_m.

6. **The Shift and Add Property:** The sum of a PN sequence and a cyclic shift of it self forms another PN sequence in the set δ_m.

7. **The Autocorrelation Property:** The autocorrelation property is the most important property, especially when the application is spread spectrum communications. This property is applied when two of the same sequences are being compared to each other. Such is the case with the received and locally generated sequences of a spread spectrum receiver. The autocorrelation function for a binary sequence $c_0c_1c_2...c_{N-\tau}$ is defined by

$$R_c(\tau) = \frac{1}{N}\sum_{j=0}^{N-1}(-1)^{c_j+c_{\tau+j}} \tag{A.6}$$

and for a NRZ sequence is defined by

$$R_c(\tau) = \frac{1}{N}\sum_{j=0}^{N-1}c_jc_{\tau+j} \qquad c_j = \pm 1 \tag{A.7}$$

The following equation may be more easily understood, and is easy to apply to both NRZ and binary sequences

$$R_c(\tau) = \frac{A-D}{N} \tag{A.8}$$

where 'A' is the number of places where the sequences agree, 'D' is the number of places where the sequences disagree, 'N' is the length of the sequence, and $A+D=N$. Application of the above equations yields the following results

$$R_c(\tau) = 1 \text{ when } \tau = \varepsilon N \text{ and } R_c(\tau) = -\frac{1}{N} \text{ when } \tau \neq \varepsilon N; \quad \text{where } \varepsilon \text{ is an integer} \tag{A.9}$$

Graphically the autocorrelation function looks like the following

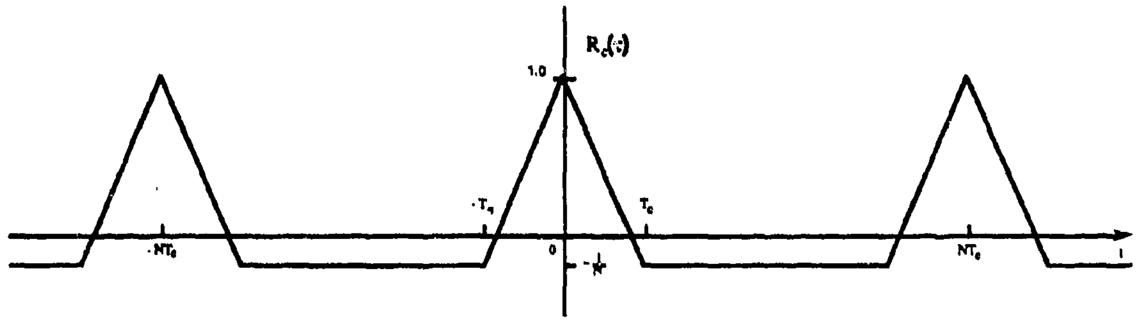


Figure A-4 Plot of the autocorrelation function. The PN waveform is periodic with triangular pulses of width $2T_c$ repeated every NT_c seconds [Ref. 1:p. 407].

In layman's terms, the autocorrelation of two identical sequences is maximum when the two sequences are perfectly aligned in phase. If they are more than $\pm T_c$ apart, the autocorrelation is $-\frac{1}{N}$.

8. **The Runs Property:** In any PN sequence, 1/2 of the runs have length 1, 1/4 have a length of 2, 1/8 have a length of 3, etc. In each case, the number of runs (repetitions) of zeros is equal to the number of runs of ones.

APPENDIX B: LINK ANALYSIS PROGRAM AND RESULTS

The following program and results are supplied with little explanation. Their inclusion is for reference only.

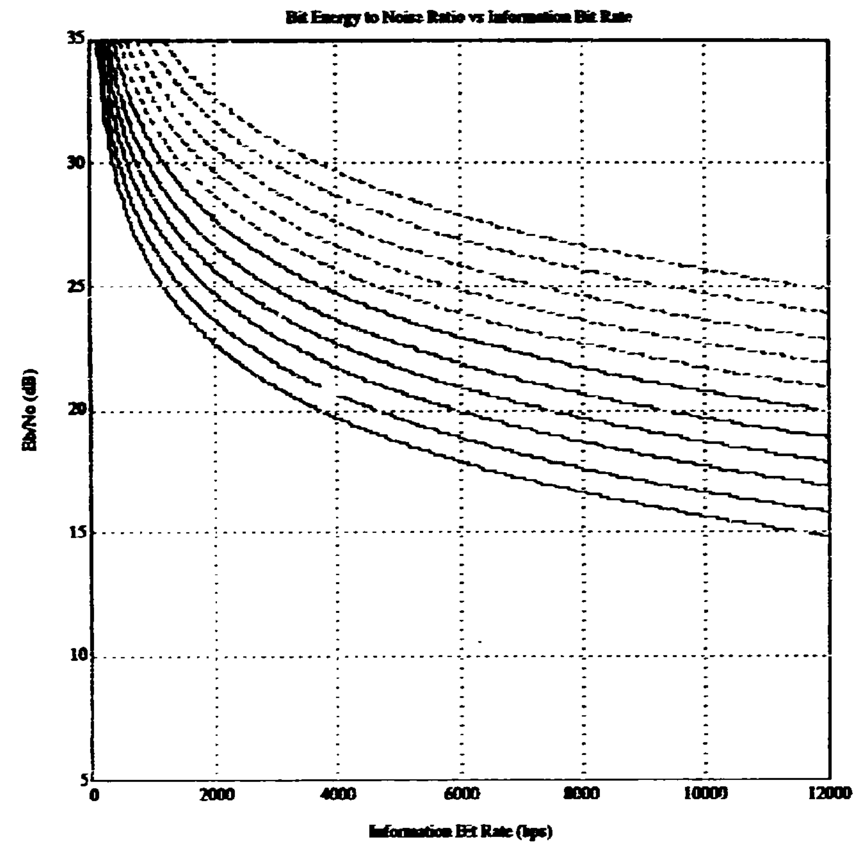


Figure B-1 Bit energy to noise ratio over a range of powers from 0.2 watts to 2.0 watts. The lowest curve is for 0.2 watts.

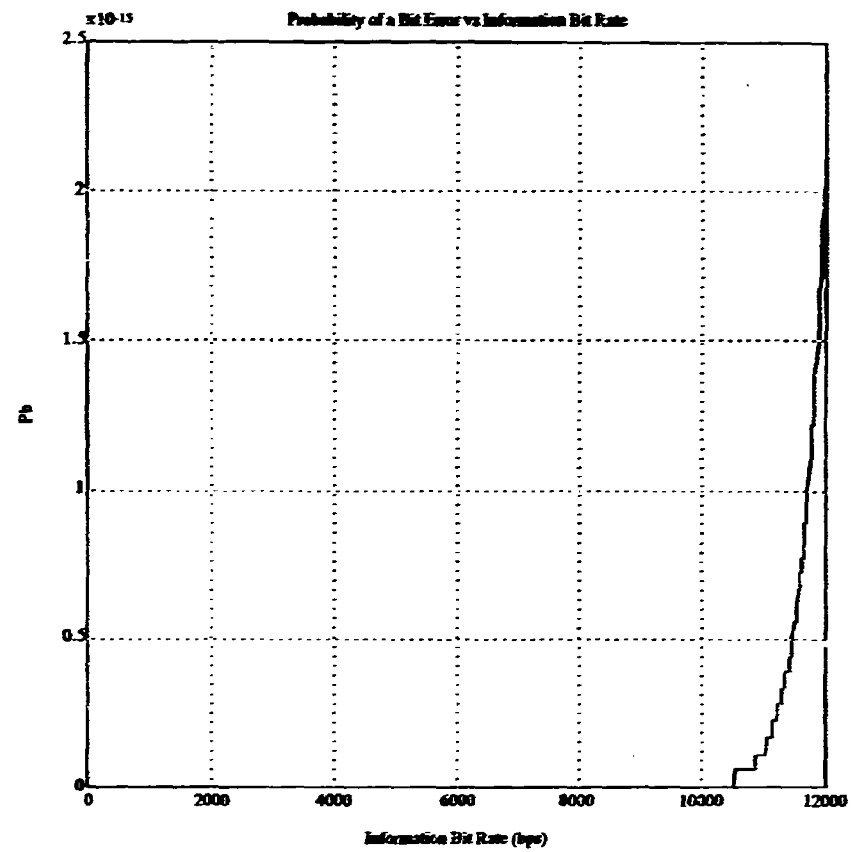


Figure B-2 Probability of a bit error vs the data rate for various levels of power. The only curve to show up on this plot is for 0.2 watts

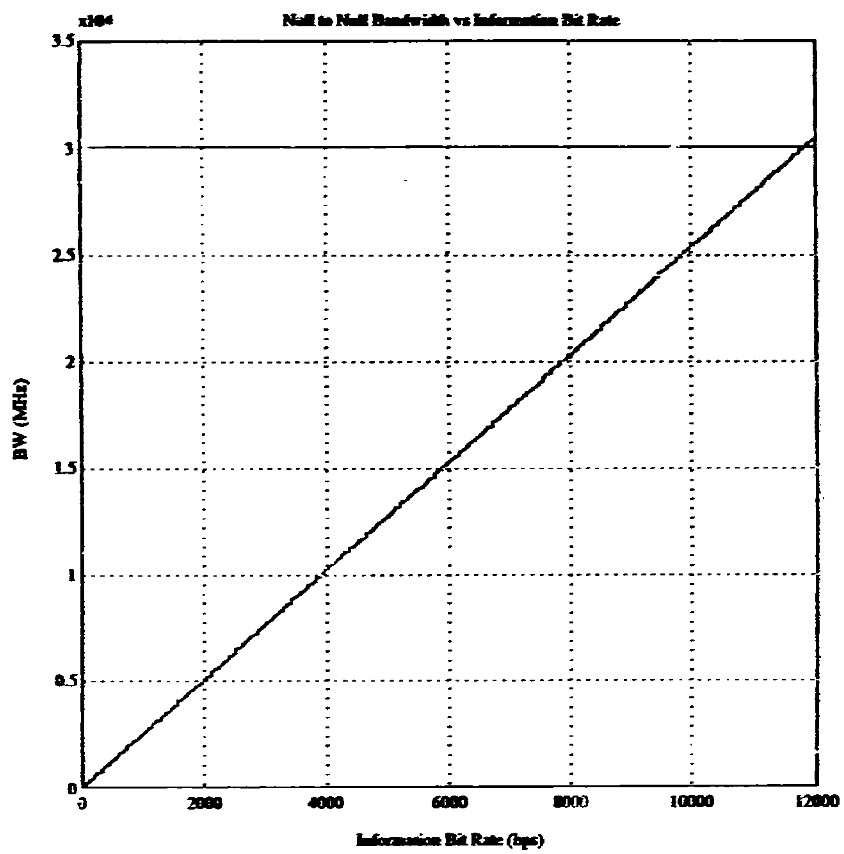


Figure B-3 Required bandwidth vs data rate. The line at 3 MHz represents a limit imposed by the FCC.

DSSS UPLINK BUDGET

Trx = 172.0360

Frx_dB = 2.0228

Tsys = 452.0360

Pt_Watts = 0.2000 0.2500 0.3200 0.4000 0.5000 0.6400 0.8000
1.0000 1.2500 1.6000 2.0000

EIRP_dBm = 35.0103 35.9794 37.0515 38.0206 38.9897 40.0618 41.0309
42.0000 42.9691 44.0412 45.0103

C_dBm = -116.3669 -115.3978 -114.3257 -113.3566 -112.3875 -111.3154 -110.3463
-109.3772 -108.4081 -107.3360 -106.3669

N_dBm = -108.0712

CN_dB = -8.2957 -7.3266 -6.2545 -5.2854 -4.3163 -3.2442 -2.2751
-1.3060 -0.3369 0.7352 1.7043

CN_at_Det_dB = 12.7424 13.7115 14.7836 15.7527 16.7218 17.7939
18.7630 19.7321 20.7012 21.7733 22.7424

EbNo_dB = 15.7527 16.7218 17.7939 18.7630 19.7321 20.8042 21.7733
22.7424 23.7115 24.7836 25.7527

Error_Prob = 0 0 0 0 0 0 0 0 0 0 0

PG = 21.0380

DSSS DOWNLINK BUDGET

Trx = 171.9809

Frx_dB = 2.0223

Tsys = 451.9809

Pt_Watts = 0.2000 0.2500 0.3200 0.4000 0.5000 0.6400 0.8000
1.0000 1.2500 1.6000 2.0000

EIRP_dBm = 23.0103 23.9794 25.0515 26.0206 26.9897 28.0618 29.0309
30.0000 30.9691 32.0412 33.0103

C_dBm = -116.3669 -115.3978 -114.3257 -113.3566 -112.3875 -111.3154 -110.3463
-109.3772 -108.4081 -107.3360 -106.3669

N_dBm = -108.0717

CN_dB = -8.2951 -7.3260 -6.2539 -5.2848 -4.3157 -3.2436 -2.2745
-1.3054 -0.3363 0.7358 1.7049

CN_at_Det_dB = 12.7429 13.7120 14.7841 15.7532 16.7223 17.7944
18.7635 19.7326 20.7017 21.7738 22.7429

EbNo_dB = 15.7532 16.7223 17.7944 18.7635 19.7326 20.8047
21.7738 22.7429 23.7120 24.7841 25.7532

Error_Prob = 0 0 0 0 0 0 0 0 0 0 0

PG = 21.0380

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%
%
% DSSS/BPSK UPLINK BUDGET :   Arnie Brown  7/14/93
%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clear
clg

Pt=[.2 .25 .32 .40 .50 .64 .80 1.0 1.25 1.60 2.0]; % tx pwr (watts)

% constants

Gain=[22.5 27 27 27];  % rx front end amplifier gains (dB)
NF=[2 1.6 1.6 1.6];    % rx amplifier noise figures (dB)
Gtx=12;                % gain of tx antenna
Grx=0;                 % gain of rx antenna
Tant=280;              % rx antenna temp due to rxvd radiation
E=5;                   % worst case ground station antenna elevation in deg
fc=436.5e6;            % carrier frequency
r=6378.155e3;          % earth radius in km
h=480e3;               % sat altitude in km
c=2.997925e8;          % speed of light
k=1.38e-23;            % Boltzmann's constant

% converting from dB

F=10 .^(NF/10);
G=10 .^(Gain/10);
Gt=10 .^(Gtx/10);
Gr=10 .^(Grx/10);

% calculation of the rx noise figure and noise temp

Frx=F(1) + F(2)/G(1) + F(3)/(G(1)*G(2)) + F(4)/(G(1)*G(2)*G(3));
Trx=290*(Frx-1);
Tsys=Tant+Trx;

% calculating the worst case slant range and free space loss

d=sqrt((r+h)^2+r^2-2*r*(r+h)*sin(E*pi/180+asin(r/(r+h)*cos(E*pi/180))));
Lfs=(4*pi*fc*d/c)^2;
```

```
% calculating IF BW for a various data rates

R=1:10:12000;
R=R';
fchip=127*R;
B=2*fchip;       % noise bandwidth

% calculation of the system noise temp and noise figure

N=k*Tsys*B;

% calculating the effective radiated pwr

for n=1:length(Pt)

eirp(n)=Pt(n)*Gt;

% calculating the received signal pwr at the satellite

 Crx(n)=eirp(n)*Gr/Lfs;

% calculating C/N and Eb/No

 CN(:,n)=Crx(n)*(ones(1:length(N)))' ./N;
 EbNo(:,n)=CN(:,n) .*B ./R;

% calculating the probability of a bit error

 Pb(:,n)=.5*(1-erf(sqrt(EbNo(:,n))));  % fcn of PSD (Eb/No) as measured at the detector input
end
EN=10*log10(EbNo);

% calculating only for 9.84 kbps

B1=2*127*9.84e3;
N1=k*Tsys*B1;
N2=k*Tsys*2*9.84e3;
CN1=Crx/N1;
CN2=Crx/N2;
EbNo1=CN1*B1/9.84e3;
Pb1=.5*(1-erf(sqrt(EbNo1)));
PG=10*log10(127);
```

```
% writing results to a file

delete link
diary link
disp('DSSS UPLINK BUDGET')
Trx,Frx_dB=10*log10(Frx),Tsys,Pt_Watts=Pt,EIRP_dBm=10*log10(eirp/1e-3),...
C_dBm=10*log10(Crx/1e-3),N_dBm=10*log10(N1/1e-3),CN_dB=10*log10(CN1),...
CN_at_Det_dB=10*log10(CN2),EbNo_dB=10*log10(EbNo1),Error_Prob=Pb1,...
PG
diary off

axis('square');
axis([0,12000,5,35]);
plot(R,EN(:,1),R,EN(:,2),R,EN(:,3),R,EN(:,4),R,EN(:,5),R,EN(:,6),...
R,EN(:,7),R,EN(:,8),R,EN(:,9),R,EN(:,10),R,EN(:,11)),...
title('Bit Energy to Noise Ratio vs Information Bit Rate'),...
xlabel('Information Bit Rate (bps)'),...
ylabel('Eb/No (dB)'),grid,pause
axis;

plot(R,Pb(:,1),R,Pb(:,2),R,Pb(:,3),R,Pb(:,4),R,Pb(:,5),R,Pb(:,6),...
R,Pb(:,7),R,Pb(:,8),R,Pb(:,9),R,Pb(:,10),R,EN(:,11)),...
title('Probability of a Bit Error vs Information Bit Rate'),...
xlabel('Information Bit Rate (bps)'),...
ylabel('Pb'),grid,pause

axis([0,12000,0,1e-6]);
plot(R,Pb(:,1),R,Pb(:,2),R,Pb(:,3),R,Pb(:,4),R,Pb(:,5),R,Pb(:,6),...
R,Pb(:,7),R,Pb(:,8),R,Pb(:,9),R,Pb(:,10),R,Pb(:,11)),...
title('Probability of a Bit Error vs Information Bit Rate'),...
xlabel('Information Bit Rate (bps)'),...
ylabel('Pb'),grid,pause
axis;

axis([0,12000,0,1e-10]);
plot(R,Pb(:,1),R,Pb(:,2),R,Pb(:,3),R,Pb(:,4),R,Pb(:,5),R,Pb(:,6),...
R,Pb(:,7),R,Pb(:,8),R,Pb(:,9),R,Pb(:,10),R,Pb(:,11)),...
title('Probability of a Bit Error vs Information Bit Rate'),...
xlabel('Information Bit Rate (bps)'),...
ylabel('Pb'),grid,pause
axis;

axis([0,12000,0,1e-13]);
```

```
plot(R,Pb(:,1),R,Pb(:,2),R,Pb(:,3),R,Pb(:,4),R,Pb(:,5),R,Pb(:,6),...
R,Pb(:,7),R,Pb(:,8),R,Pb(:,9),R,Pb(:,10),R,Pb(:,11)),...
title('Probability of a Bit Error vs Information Bit Rate'),...
xlabel('Information Bit Rate (bps)'),...
ylabel('Pb'),grid,pause
axis;

axis('square');
plot(R,B,R,3e6*ones(1:length(R))),...
title('Null to Null Bandwidth vs Information Bit Rate'),...
xlabel('Information Bit Rate (bps)'),
ylabel('BW (MHz)'),grid
```

APPENDIX C: GENERALIZED IMPEDANCE CONVERTER (GIC) FILTER DESIGN PROGRAM

The following program was based on notes written by Professor Micheal at the Naval Postgraduate School, and was written with help from CAPT. Bing Bingham, USMC. This program was used to design the BPFs in Costas loop on board 4. It provides magnitude plots, phase plots, and component values. A component value is computed for each of the variables shown in the following figure.

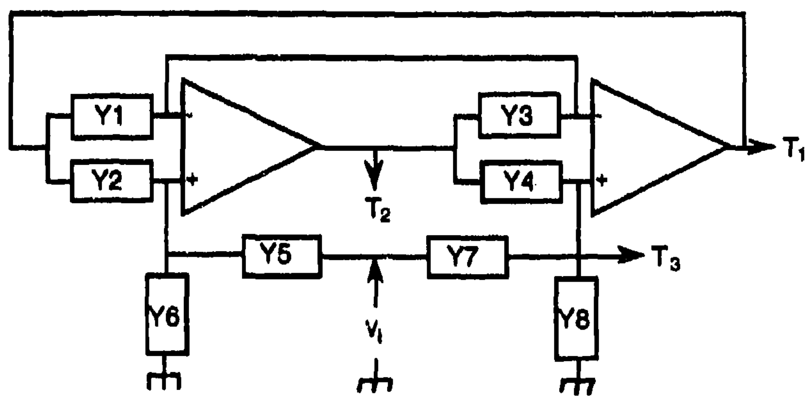


Figure C-1 GIC filter topology

The transfer function for the above topology is

$$T(s) = \frac{N(s)}{D(s)} \tag{C.1}$$

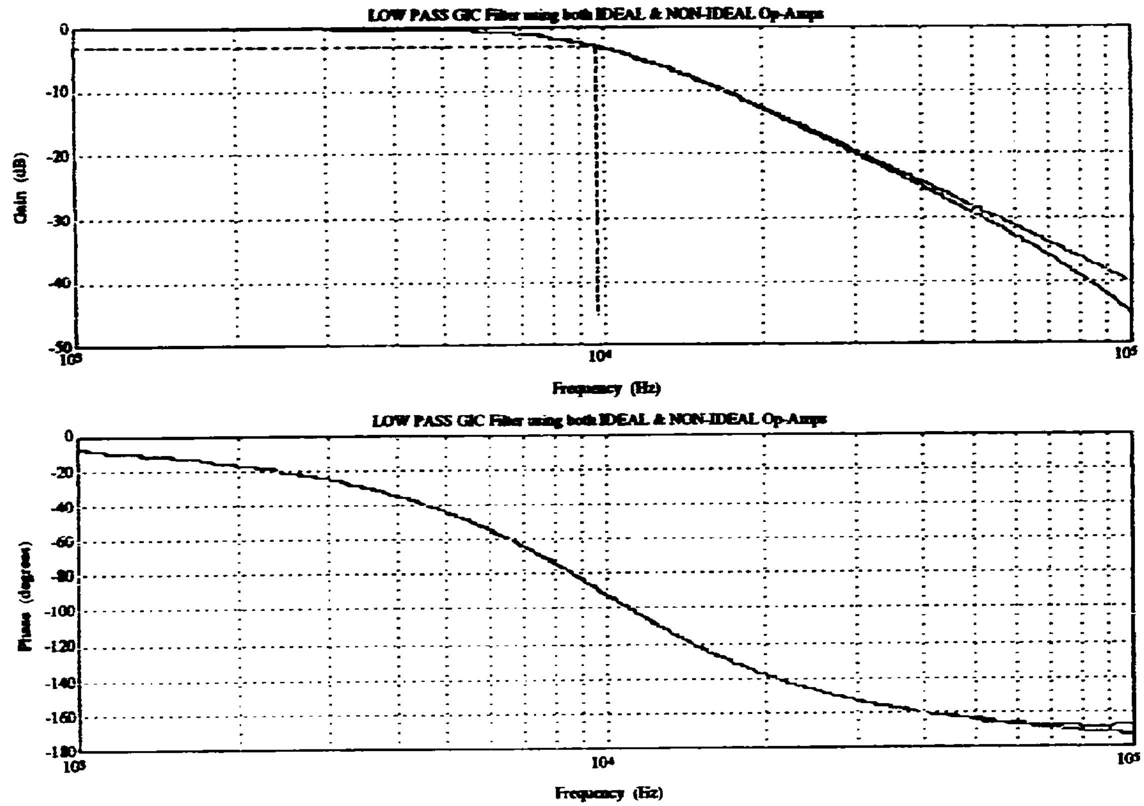
$$D(s) = s^2 + \left(\frac{\omega_p}{Q_p}\right)s + \omega_p^2 \tag{C.2}$$

Each filter type has its own transfer function. A list of the filter types and its corresponding variable equations and transfer function is provided in Table C-1. This table is provided for clarity. It is not necessary for the proper operation of the program, but the following equations are

$$C = \frac{1}{R\omega} \text{ and } G = \frac{1}{R} \tag{C.3}$$

Filter Type	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Transfer Function
LP	G	C	C+1/QR	G	G	0	0	G	$T_2 = \frac{2\omega_p^2}{D(s)}$
HP	G	G	C	G	0	G	C	1/QR	$T_1 = \frac{2s^2}{D(s)}$
BP	G	G	C	G	0	G	1/QR	C	$T_1 = \frac{2\left(\frac{\omega_p}{Q_p}\right)^2}{D(s)}$
N	G	G	C	G	G	0	C	1/QR	$T_2 = \frac{(s^2+\omega_p^2)}{D(s)}$
AP	G	G	C	G	G	0	C	1/QR	$T_1 = \frac{\left(s^2 - \frac{\omega_p}{Q_p}s + \omega_p^2\right)}{D(s)}$

Table C-1: GIC filter transfer function and variable equations for the various filter types



Y1_ohms =	10000
Y2_farads =	1.6174e-09
Y3a_farads =	1.6174e-09
Y3b_ohms =	7.0700e+03
Y4_ohms =	10000
Y5_ohms =	10000
Y6 =	0
Y7 =	0
Y8_ohms =	10000

Output is at T2

Figure C-2 Costas loop LPF design for a cutoff frequency of 9.84 kHz. Magnitude plot, phase plot, and component values were computed using the GIC program.

```
% GIC Realization for both Ideal and Nonideal Op Amps
%
% 2 Jul 93    Arnie Brown
%
% This m-file (gic.m) uses the following "m files" writen by Bing Bingham
% and later modified by Arnie Brown:
%
%    1) addpoly.m     adds to polynomials
%    2) ideal.m       bode plots the ideal opamp
%    3) nonideal.m    bode plots the nonideal opamp
%    4) plotboth.m    bode plots the nonideal over the ideal bode
%
% ALL four of these m-files are needed to run GIC.M.
%
% This m-file is patterned after the GIC network from page 28 of
% Professor Micheal's notes.
clc
flag = 1;
while flag == 1

k=menu('Choose a Filter type','Low Pass','High Pass','Band Pass','Notch','All Pass','Exit GIC Program');

  if k == 1
    clc
r=input('Enter the input resistance:  ');
    fc=input('Enter the cutoff frequence:  ');
    Q=input('Enter the quality factor (Q):  ');
    c=1/(r*2*pi*fc);
    y1=1/r;
    y2=[c 0];
    y3=addpoly(y2,1/(r*Q));
    y4=y1;
    y5=y1;
    y6=0;
    y7=0;
    y8=y1;
delete LP
diary LP
Y1_ohms=r,Y2_farads=c,Y3a_farads=c,Y3b_ohms=(r*Q),Y4_ohms=r,Y5_ohms=r,Y6=0,...
Y7=0,Y8_ohms=r,disp('Output is at T2')
diary off
pause
    clc
```

```
p=menu('Choose IDEAL or NONIDEAL Bode plots or BOTH','IDEAL','NONIDEAL','BOTH');

    clc
    if p==1
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y1,conv(y5,y8)),...
    addpoly(conv(y2,conv(y3,y7)),((-1)*conv(y1,conv(y6,y7))))));
      idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
    addpoly(y7,y8))));
      ideal(idealnum,idealden,k)

    elseif p==2
      wt1=input('Input the Gain-Band-Width-Product for the Op-Amps:  ');
      wt2=wt1;
      nonidealnum1=addpoly(conv(y2,conv(y3,y7)),addpoly(conv(y1,conv(y5,...
       addpoly(y4,y8))),((-1)*(conv(y1,conv(y6,y7))))));
nonidealnum2=(conv(conv(y5,conv(addpoly(y1,y3),addpoly(y4,...
       addpoly(y7,y8)))),[1 0]))/wt2;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
      nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
       addpoly(y5,y6))));
      nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
       addpoly(y5,y6)))),[1 0]))/(wt1));
      nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
       addpoly(y5,y6)))),[1 0]))/(wt2));
      nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
       addpoly(y2,addpoly(y5,y6)))),[1 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
      addpoly(nonidealden3,nonidealden4)));
nonideal(nonidealnum,nonidealden,k);

      elseif p==3
      idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y1,conv(y5,y8)),...
    addpoly(conv(y2,conv(y3,y7)),((-1)*conv(y1,conv(y6,y7))))));
      idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
    addpoly(y7,y8))));
      wt1=input('Input the Gain-Band-Width-Product for the Op-Amps:  ');
      wt2=wt1;
      nonidealnum1=addpoly(conv(y2,conv(y3,y7)),addpoly(conv(y1,conv(y5,...
       addpoly(y4,y8))),((-1)*(conv(y1,conv(y6,y7))))));
nonidealnum2=(conv(conv(y5,conv(addpoly(y1,y3),addpoly(y4,...
       addpoly(y7,y8)))),[1 0]))/wt2;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
      nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
```

```
         addpoly(y5,y6))));
        nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt1));
        nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt2));
        nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
         addpoly(y2,addpoly(y5,y6)))),[1 0 0]))/(wt1*wt2));
 nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
        addpoly(nonidealden3,nonidealden4)));
 plotboth(idealnum,idealden,nonidealnum,nonidealden,k);

      end

   elseif k == 2
     clc
     r=input('Enter the value of input resistance:  ');
     fc=input('Enter the cutoff frequence:  ');
     c=1/(r*2*pi*fc);
     Q=input('Enter the quality factor (Q):  ');
     y1=1/r;
     y2=y1;
     y3=[c 0];
     y4=y1;
     y5=0;
     y6=y1;
     y7=y3;
     y8=1/(r*Q);
delete HP
diary HP
Y1_ohms=r,Y2_ohms=r,Y3_farads=c,Y4_ohms=r,Y5=0,Y6_ohms=r,Y7_farads=c,...
Y8_ohms=(r*Q),
disp('Output is at T1')
diary off
pause
    clc
    p=menu('Choose IDEAL or NONIDEAL Bode plots or BOTH','IDEAL','NONIDEAL','BOTH');
      clc
      if p==1
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
      addpoly(y2,y6))),((-1) * conv(y3,conv(y5,y8)))));
        idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
      addpoly(y7,y8))));
ideal(idealnum,idealden,k);
```

```
elseif p==2
  wt1=input('Input the Gain-Band-Width-Product for the OpAmps: ');
  wt2=wt1;
  nonidealnum1=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
   addpoly(y2,y6))),((-1)*(conv(y3,conv(y5,y8))))));
nonidealnum2=(conv(conv(y7,conv(addpoly(y1,y3),addpoly(y2,...
   addpoly(y5,y6)))),[1 0]))/wt1;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
  nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
   addpoly(y5,y6))));
  nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
   addpoly(y5,y6)))),[1 0]))/(wt1));
  nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
   addpoly(y5,y6)))),[1 0]))/(wt2));
  nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
   addpoly(y2,addpoly(y5,y6)))),[1 0 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
  addpoly(nonidealden3,nonidealden4)));
nonideal(nonidealnum,nonidealden,k);
 elseif p==3
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
 addpoly(y2,y6))),((-1) * conv(y3,conv(y5,y8)))));
  idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
 addpoly(y7,y8))));
  wt1=input('Input the Gain-Band-Width-Product for the OpAmps: ');
  wt2=wt1;
  nonidealnum1=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
   addpoly(y2,y6))),((-1)*(conv(y3,conv(y5,y8))))));
nonidealnum2=(conv(conv(y7,conv(addpoly(y1,y3),addpoly(y2,...
   addpoly(y5,y6)))),[1 0]))/wt1;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
  nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
   addpoly(y5,y6))));
  nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
   addpoly(y5,y6)))),[1 0]))/(wt1));
  nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
   addpoly(y5,y6)))),[1 0]))/(wt2));
  nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
   addpoly(y2,addpoly(y5,y6)))),[1 0 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
  addpoly(nonidealden3,nonidealden4)));
plotboth(idealnum,idealden,nonidealnum,nonidealden,k);
 end
```

```
elseif k == 3
  clc
  r=input('Enter the value of input resistance:  ');
  fc=input('Enter the center frequence (Hz):  ');
  B=input('Enter the 3dB bandwidth (Hz):  ');
  c=1/(r*2*pi*fc);
  Q=fc/B;
  y1=1/r;
  y2=y1;
  y3=[c 0];
  y4=y1;
  y5=0;
  y6=y1;
  y7=1/(r*Q);
  y8=y3;
delete BP
diary BP
Y1_ohms=r,Y2_ohms=r,Y3_farads=c,Y4_ohms=r,Y5=0,Y6_ohms=r,Y7_ohms=(r*Q),...
Y8_farads=c,
disp('Output is at T1'),Q,
diary off
pause
  clc
  p=menu('Choose IDEAL or NONIDEAL Bode plots or BOTH','IDEAL','NONIDEAL','BOTH');
   clc
   if p==1
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
   addpoly(y2,y6))),((-1) * conv(y3,conv(y5,y8)))));
     idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
   addpoly(y7,y8))));
ideal(idealnum,idealden,k);
   elseif p==2
     wt1=input('Input the Gain-Band-Width-Product for the Op-Amps:  ');
     wt2=wt1;
     nonidealnum1=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
      addpoly(y2,y6))),((-1)*(conv(y3,conv(y5,y8))))));
nonidealnum2=(conv(conv(y7,conv(addpoly(y1,y3),addpoly(y2,...
      addpoly(y5,y6)))),[1 0]))/wt1;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
     nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
      addpoly(y5,y6))));
     nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
```

```
          addpoly(y5,y6)))),[1 0]))/(wt1));
          nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
          addpoly(y5,y6)))),[1 0]))/(wt2));
          nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
          addpoly(y2,addpoly(y5,y6)))),[1 0 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
          addpoly(nonidealden3,nonidealden4)));
nonideal(nonidealnum,nonidealden,k);
      elseif p==3
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
      addpoly(y2,y6))),((-1) * conv(y3,conv(y5,y8)))));
        idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
      addpoly(y7,y8))));
        wt1=input('Input the Gain-Band-Width-Product for the OpAmps: ');
        wt2=wt1;
        nonidealnum1=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
         addpoly(y2,y6))),((-1)*(conv(y3,conv(y5,y8))))));
nonidealnum2=(conv(conv(y7,conv(addpoly(y1,y3),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/wt1;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
        nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
         addpoly(y5,y6))));
        nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt1));
        nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt2));
        nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
         addpoly(y2,addpoly(y5,y6)))),[1 0 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
        addpoly(nonidealden3,nonidealden4)));
plotboth(idealnum,idealden,nonidealnum,nonidealden,k);
      end

  elseif k == 4
    clc
    r=input('Enter the value of input resistance: ');
    fc=input('Enter the center frequence: ');
    B=input('Enter the 3dB bandwidth: ');
    c=1/(r*2*pi*fc);
    Q=fc/B;
    y1=1/r;
    y2=y1;
    y3=[c 0];
```

```
    y4=y1;
    y5=y1;
    y6=0;
    y7=y3;
    y8=1/(r*Q);
delete N
diary N
Y1_ohms=r,Y2_ohms=r,Y3_farads=c,Y4_ohms=r,Y5_ohms=r,Y6=0,Y7_farads=c,...
Y8_ohms=(r*Q),
disp('Output is at T2'),Q
diary off
pause
    clc
    p=menu('Choose IDEAL or NONIDEAL Bode plots or BOTH','IDEAL','NONIDEAL','BOTH');
      clc
      if p==1
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y1,conv(y5,y8)),...
      addpoly(conv(y2,conv(y3,y7)),((-1)*conv(y1,conv(y6,y7))))));
        idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
      addpoly(y7,y8))));
ideal(idealnum,idealden,k);
      elseif p==2
        wt1=input('Input the Gain-Band-Width-Product for the OpAmps: ');
        wt2=wt1;
        nonidealnum1=addpoly(conv(y2,conv(y3,y7)),addpoly(conv(y1,conv(y5,...
         addpoly(y4,y8))),((-1)*(conv(y1,conv(y6,y7))))));
nonidealnum2=(conv(conv(y5,conv(addpoly(y1,y3),addpoly(y4,...
         addpoly(y7,y8)))),[1 0]))/wt2;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
        nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
         addpoly(y5,y6))));
        nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt1));
        nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt2));
        nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
         addpoly(y2,addpoly(y5,y6)))),[1 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
        addpoly(nonidealden3,nonidealden4)));
nonideal(nonidealnum,nonidealden,k);
      elseif p==3
        idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y1,conv(y5,y8)),...
      addpoly(conv(y2,conv(y3,y7)),((-1)*conv(y1,conv(y6,y7))))));
```

```
        idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
       addpoly(y7,y8))));
        wt1=input('Input the Gain-Band-Width-Product for the OpAmps: ');
        wt2=wt1;
        nonidealnum1=addpoly(conv(y2,conv(y3,y7)),addpoly(conv(y1,conv(y5,...
         addpoly(y4,y8))),((-1)*(conv(y1,conv(y6,y7))))));
nonidealnum2=(conv(conv(y5,conv(addpoly(y1,y3),addpoly(y4,...
         addpoly(y7,y8)))),[1 0]))/wt2;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
        nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
         addpoly(y5,y6))));
        nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt1));
        nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
         addpoly(y5,y6)))),[1 0]))/(wt2));
        nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
         addpoly(y2,addpoly(y5,y6)))),[1 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
        addpoly(nonidealden3,nonidealden4)));
plotboth(idealnum,idealden,nonidealnum,nonidealden,k);
      end

  elseif k == 5
    clc
    r=input('Enter the value of input resistance: ');
    fc=input('Enter the center frequence: ');
    Q=input('Enter the value of Quality factor (Q): ');
    c=1/(r*2*pi*fc);
    y1=1/r;
    y2=y1;
    y3=[c 0];
    y4=y1;
    y5=y1;
    y6=0;
    y7=y3;
    y8=1/(r*Q);
delete AP
diary AP
Y1_ohms=r,Y2_ohms=r,Y3_farads=c,Y4_ohms=r,Y5_ohms=r,Y6=0,Y7_farads=c,...
Y8_ohms=1/y8,
disp('Output is at T1')
diary off
pause
```

```
clc
p=menu('Choose IDEAL or NONIDEAL Bode plots or BOTH','IDEAL','NONIDEAL','BOTH');
 clc
 if p==1
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
    addpoly(y2,y6))),((-1) * conv(y3,conv(y5,y8)))));
      idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
    addpoly(y7,y8))));
ideal(idealnum,idealden,k);
    elseif p==2
      wt1=input('Input the Gain-Band-Width-Product for the Op-Amps: ');
      wt2=wt1;
      nonidealnum1=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
       addpoly(y2,y6))),((-1)*(conv(y3,conv(y5,y8))))));
nonidealnum2=(conv(conv(y7,conv(addpoly(y1,y3),addpoly(y2,...
       addpoly(y5,y6)))),[1 0]))/wt1;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
      nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
       addpoly(y5,y6))));
      nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
       addpoly(y5,y6)))),[1 0]))/(wt1));
      nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
       addpoly(y5,y6)))),[1 0]))/(wt2));
      nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
       addpoly(y2,addpoly(y5,y6)))),[1 0 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
      addpoly(nonidealden3,nonidealden4)));
nonideal(nonidealnum,nonidealden,k);
    elseif p==3
idealnum=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
    addpoly(y2,y6))),((-1) * conv(y3,conv(y5,y8)))));
      idealden=addpoly(conv(y1,conv(y4,addpoly(y5,y6))),conv(y2,conv(y3,...
    addpoly(y7,y8))));
      wt1=input('Input the Gain-Band-Width-Product for the Op-Amps: ');
      wt2=wt1;
      nonidealnum1=addpoly(conv(y1,conv(y4,y5)),addpoly(conv(y3,conv(y7,...
       addpoly(y2,y6))),((-1)*(conv(y3,conv(y5,y8))))));
nonidealnum2=(conv(conv(y7,conv(addpoly(y1,y3),addpoly(y2,...
       addpoly(y5,y6)))),[1 0]))/wt1;
nonidealnum=addpoly(nonidealnum1,nonidealnum2);
      nonidealden1=addpoly(conv(y2,conv(y3,addpoly(y7,y8))),conv(y1,conv(y4,...
       addpoly(y5,y6))));
      nonidealden2=((conv(conv(y1,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
```

```
        addpoly(y5,y6)))),[1 0]))/(wt1));
        nonidealden3=((conv(conv(y3,conv(addpoly(y4,addpoly(y7,y8)),addpoly(y2,...
        addpoly(y5,y6)))),[1 0]))/(wt2));
        nonidealden4=((conv(conv(addpoly(y1,y3),conv(addpoly(y4,addpoly(y7,y8)),...
        addpoly(y2,addpoly(y5,y6)))),[1 0 0]))/(wt1*wt2));
nonidealden=addpoly(nonidealden1,addpoly(nonidealden2,...
        addpoly(nonidealden3,nonidealden4)));
plotboth(idealnum,idealden,nonidealnum,nonidealden,k);
      end

  elseif k == 6;
    break;

  elseif k == 99;
    keyboard;

  end

end

function y=addpoly(a,b)
%
% EC4100                        Bing Bingham
%
% Network Theory                Dr. Sherif Michael
%
%               21 Aug 92
%
% This function adds two polynomials together after ensuring
% that they have same length so as not to lose their correct
% exponent value.  Different length polynomials are zero
% padded.
%
%

if length(a) >= length(b)
  b=[zeros(1,length(a) - length(b)) b];
else
  a=[zeros(1,length(b) - length(a)) a];
end

y = a+b;
```

```
function y=ideal(idealnum,idealden,k)
%
% 2 Jul 93  Arnie Brown
%
% This function draws the bode plots for an ideal op-amp.
%
% "k" is obtained from the opening menu and is passed in.
%
clc
f1=input('Enter the BEGINNING frequency for the bode plot in powers of 10 (1Hz=0):  ');
f2=input('Enter the ENDING frequency for the bode plot in powers of 10 (100MHz=8):  ');
f=logspace(f1,f2,500);
clc;clg
[idealmag,idealphase]=bode(idealnum,idealden,2*pi*f);
idealmag=idealmag/max(idealmag);
if k==1
  subplot(211)
  x=find(idealmag>.707);
  semilogx(f,20*log10(idealmag),f(1:max(x)),-3*ones(1:max(x)),...
  [f(max(x)) f(max(x))],[min(20*log10(idealmag)) -3],'g'),grid;
  title('Magnitude Plot for a LOW PASS GIC Filter using IDEAL Op-Amps');
elseif k==2
  subplot(211)
  x=find(idealmag>.707);
  semilogx(f,20*log10(idealmag),...
  f(x),-3*ones(x),...
  [f(min(x)) f(min(x))],[min(20*log10(idealmag)) -3],'g'),grid;
  title('Magnitude Plot for a LOW PASS GIC Filter using IDEAL Op-Amps');
elseif k==3
  subplot(211)
  x=find(idealmag>.707);
  semilogx(f,20*log10(idealmag),...
  [f(min(x)) f(min(x))],[min(20*log10(idealmag)) -3],...
  [f(max(x)) f(max(x))],[min(20*log10(idealmag)) -3],'g',...
  f(x),-3*ones(1:length(x)),'g'),grid;
  title('Magnitude Plot for a BAND PASS GIC Filter using IDEAL Op-Amps');
elseif k==4
  subplot(211)
  semilogx(f,20*log10(idealmag)),grid;
  title('Magnitude Plot for a NOTCH GIC Filter using IDEAL Op-Amps');
elseif k==5
  subplot(211)
  semilogx(f,20*log10(idealmag)),grid;
```

```
  title('Magnitude Plot for a ALL PASS GIC Filter using IDEAL Op-Amps');
end
xlabel('Frequency  (Hz)');ylabel('Gain  (dB)');
subplot(212);
semilogx(f,idealphase),grid;
if k==1
  title('Phase Plot for a LOW PASS GIC Filter using IDEAL Op-Amps');
elseif k==2
  title('Phase Plot for a HIGH PASS GIC Filter using IDEAL Op-Amps');
elseif k==3
  title('Phase Plot for a BAND PASS GIC Filter using IDEAL Op-Amps');
elseif k==4
  title('Phase Plot for a NOTCH GIC Filter using IDEAL Op-Amps');
elseif k==5
  title('Phase Plot for a ALL PASS GIC Filter using IDEAL Op-Amps');
end
xlabel('Frequency  (Hz)');
ylabel('Phase  (degrees)');
pause;

function y=nonideal(nonidealnum,nonidealden,k)
%
% This function draws the bode plots for an nonideal opamp
%
% "k" is obtained from the opening menu and is passed in.
%
clc
f1=input('Enter the BEGINNING frequency for the bode plot in powers of 10 (1Hz=0)  ');
f2=input('Enter the ENDING frequency for the bode plot in powers of 10 (100MHz=8)  ');
f=logspace(f1,f2,500);
clc;clg
[nonidealmag,nonidealphase]=bode(nonidealnum,nonidealden,2*pi*f);
nonidealmag=nonidealmag/max(nonidealmag);
if k==1
  subplot(211)
  x=find(nonidealmag>.707);
  semilogx(f,20*log10(nonidealmag),f(1:max(x)),-3*ones(1:max(x)),...
  [f(max(x)) f(max(x))],[min(20*log10(nonidealmag)) -3],'g'),grid;
  title('Magnitude Plot for a LOW PASS GIC Filter using NONIDEAL Op-Amps');
elseif k==2
  subplot(211)
  x=find(nonidealmag>.707);
  semilogx(f,20*log10(nonidealmag),...
```

```
    f(min(x):length(nonidealmag)),-3*ones(min(x):length(nonidealmag)),...
    [f(min(x)) f(min(x))],[min(20*log10(nonidealmag)) -3],'g'),grid;
    title('Magnitude Plot for a LOW PASS GIC Filter using NONIDEAL Op-Amps');
  elseif k==3
    subplot(211)
    x=find(nonidealmag>.707);
    semilogx(f,20*log10(nonidealmag),...
    [f(min(x)) f(min(x))],[min(20*log10(nonidealmag)) -3],...
    [f(max(x)) f(max(x))],[min(20*log10(nonidealmag)) -3],'g',...
    f(x),-3*ones(1:length(x)),'g'),grid;
    title('Magnitude Plot for a BAND PASS GIC Filter using NONIDEAL Op-Amps');
  elseif k==4
    subplot(211)
    semilogx(f,20*log10(nonidealmag)),grid;
    title('Magnitude Plot for a NOTCH GIC Filter using NONIDEAL Op-Amps');
  elseif k==5
    subplot(211)
    semilogx(f,20*log10(nonidealmag)),grid;
    title('Magnitude Plot for a ALL PASS GIC Filter using NONIDEAL Op-Amps');
end
xlabel('Frequency  (Hz)');ylabel('Gain  (dB)');
subplot(212);
semilogx(f,nonidealphase),grid;
if k==1
  title('Phase Plot for a LOW PASS GIC Filter using NONIDEAL Op-Amps');
elseif k==2
  title('Phase Plot for a HIGH PASS GIC Filter using NONIDEAL Op-Amps');
elseif k==3
  title('Phase Plot for a BAND PASS GIC Filter using NONIDEAL Op-Amps');
elseif k==4
  title('Phase Plot for a NOTCH GIC Filter using NONIDEAL Op-Amps');
elseif k==5
end
xlabel('Frequency  (Hz)');
ylabel('Phase  (degrees)');
pause;

function y=plotboth(num,DEN,NUM,DENN,k)
%
% 2 Jul 93  Arnie Brown
%
% This function draws the bode plots for an both ideal and non-ideal op-amps.
%
```

```
% "k" is obtained from the opening menu and is passed in.
%
clc
f1=input('Enter the BEGINNING frequency for the bode plot in powers of 10 (1Hz=0)  ');
f2=input('Enter the ENDING frequency for the bode plot in powers of 10 (100MHz=8)  ');
f=logspace(f1,f2,500);
clc
clg
[idealmag,idealphase]=bode(num,DEN,2*pi*f);
idealmag=idealmag/max(idealmag);
[nonidealmag,nonidealphase]=bode(NUM,DENN,2*pi*f);
nonidealmag=nonidealmag/max(nonidealmag);

if k==1
  x=find(idealmag>.707);
  subplot(211);
  semilogx(f,20*log10(idealmag),f,20*log10(nonidealmag),'b',...
  [f(max(x)) f(max(x))],[min(20*log10(nonidealmag)) -3],...
  f(1:max(x)),-3*ones(1:max(x)),'g'),grid;
  title('LOW PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==2
  x=find(idealmag>.707);
  subplot(211);
  semilogx(f,20*log10(idealmag),f,20*log10(nonidealmag),'b',...
  f(min(x):length(nonidealmag)),-3*ones(min(x):length(nonidealmag)),...
  [f(min(x)) f(min(x))],[min(20*log10(nonidealmag)) -3],'g'),grid;
  title('HIGH PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==3
  x=find(idealmag>.707);
  subplot(211);
  semilogx(f,20*log10(idealmag),f,20*log10(nonidealmag),'b',...
  [f(min(x)) f(min(x))],[min(20*log10(nonidealmag)) -3],...
  [f(max(x)) f(max(x))],[min(20*log10(nonidealmag)) -3],'g',...
  f(x),-3*ones(1:length(x)),'g'),grid;
  title('BAND PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==4
  x=find(idealmag>.707);
  subplot(211);
  semilogx(f,20*log10(idealmag),f,20*log10(nonidealmag),'b'),grid;
  title('4th Order BAND PASS GIC Filter using NON-IDEAL Op-Amps');
  xlabel('Frequency  (Hz)');
  ylabel('Gain  (dB)');
  subplot(212)
```

```
  semilogx(f,idealphase,f,nonidealphase,'b'),grid,pause,clg;
  nonidnum=conv(num,NUM);nonidden=conv(DEN,DENN);
  [nonidmag,nonidphase]=bode(nonidnum,nonidden,2*pi*f);
  nonidmag=nonidmag/max(nonidmag);
  semilogx(f,20*log10(nonidmag),...
  [f(min(x)) f(min(x))],[min(20*log10(nonidmag)) -3],...
  [f(max(x)) f(max(x))],[min(20*log10(nonidmag)) -3],'g',...
  f(x),-3*ones(1:length(x)),'g'),grid;
  subplot(212)
  semilogx(f,nonidphase),grid,pause,clg;
elseif k==5
  subplot(211)
  semilogx(f,20*log10(idealmag),f,20*log10(nonidealmag),'b')
  title('NOTCH GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==6
  subplot(211)
  semilogx(f,20*log10(idealmag),f,20*log10(nonidealmag),'b')
  title('ALL PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
end
xlabel('Frequency  (Hz)');
ylabel('Gain  (dB)');
subplot(212)
semilogx(f,idealphase,f,nonidealphase,'b'),grid;
if k==1
  title('LOW PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==2
  title('HIGH PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==3
  title('BAND PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==4
  title('NOTCH GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
elseif k==5
  title('ALL PASS GIC Filter using both IDEAL & NON-IDEAL Op-Amps');
end
xlabel('Frequency  (Hz)');
ylabel('Phase  (degrees)');
pause;
```

APPENDIX D: DESCRIPTION OF CIRCUIT SCHEMATICS

All the circuit schematics, board layouts, and routing were done on an Apple® Macintosh using a CAD/CAM system by Douglas Electronics. The RF boards described in this section where fabricated using an LPKF circuit board plotting (CBP) CAM system.

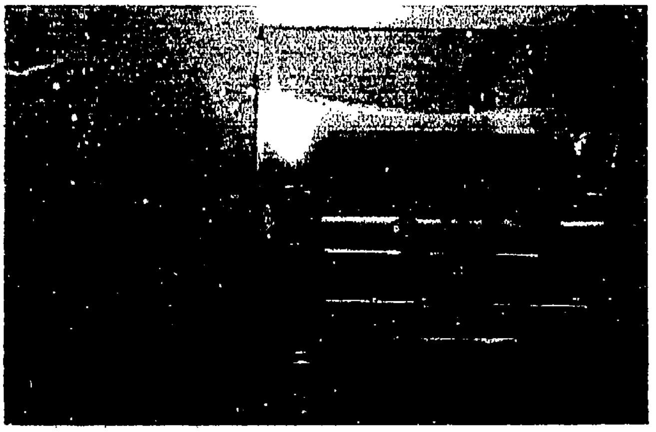


Figure D-1 LPKF Circuit Board Plotting (CBP) CAM System.

This machine mills around pads and traces to isolate them on a copper clad board. The excess copper of both the component and solder sides have been used to form a signal ground plane.

A. BOARD 1: TRANSMITTER AND RECEIVER FRONT END

Board 1 was not milled because all the components have SMA connectors on their input and output. Connections made in this way avoided high frequency circuit board design problems, and made component placement less critical. Though the design is fairly straight forward, there are still a few areas of concern such as the PIN diode switch (U2), preselection filter (U3), and the power amplifier (U4).

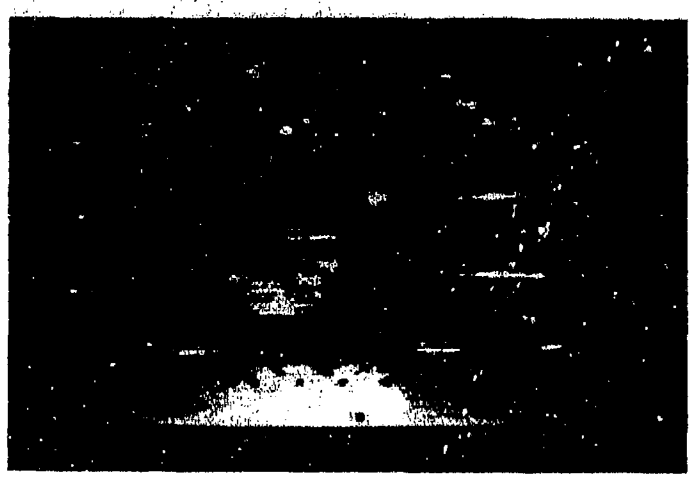


Figure D-2 RF bread board of the transmitter and receiver front end.

The PIN diode switch (U2) allows the user to select between two separate transmitters and two separate receivers. However, the component chosen has some limitations. The first limitation is a 1 dB compression point of 19 dBm and a maximum RF power of 28 dBm. Above 19 dBm the diodes will start to distort the signal, and above 28 dBm damage to the device may occur. Second limitation, it is unclear from the data sheet whether the switch is absorptive or reflective. If the device is absorptive, a port that is switched off will appear as a 50Ω load, and if it is reflective it may appear as a short [Ref. 8:p. 13-3 to 13-4]. Obviously, the absorptive case is the desirable one in this application. Of course, this should be measured before using the switch in a live circuit. The next area of concern is the high power amplifier (U4). This device was chosen because it was readily available from one of the labs here, and its maximum output power is not as likely to damage the PIN diode switch (U2). The last area of concern is the preselection filter (U3). This filter is intended to limit the band of frequencies that are allowed to enter the low noise amplifier.

It may not be necessary, but was included to eliminate strong out of band carriers that could possibly saturate the low noise amplifier.

B. BOARD 2: RECEIVER IF AMPLIFICATION, AGC, AND DETECTOR

Figure D-3 RF bread board of the Rx IF amplification, AGC, and detection circuits of board 2.

1. Rx IF Amplification and AGC Circuit

The purpose of this circuit is to provide a relatively constant amplitude wideband signal to the detector, tracker, and demodulator circuits. U1, U2, U4, and U9 supply the gain, while U6 attempts to maintain a constant amplitude signal. U6 is an AGC amplifier with a 0-5 volt control voltage. Its feedback control voltage is developed with U11, U12, and U7. U11 provides a portion of the signal power to U12, the analog level detector, without causing reflections on the main signal path. U12 contains both reference and detector diodes, as shown in the figure below.

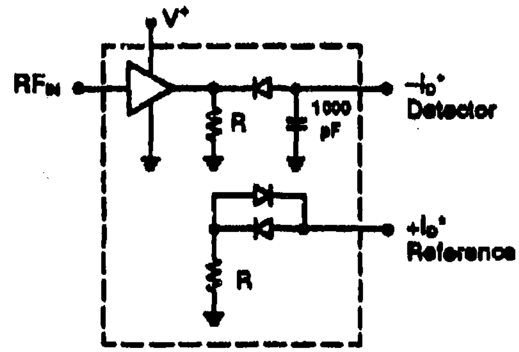
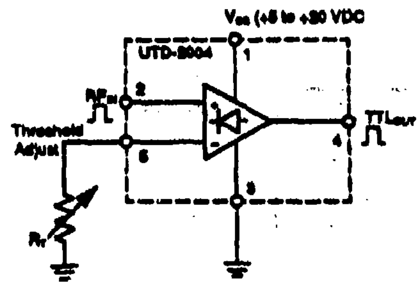


Figure D-4 Schematic diagram of the analog level detector (U12) [Ref. 6:p. (5-10)].

These diodes are provided a bias current to increase their sensitivity. The biasing is cancelled out by summing the detectors output with the reference. The AGC amplifier is capable of providing both gain and attenuation, leading to a range of over 36 dB. When the signal power applied to the input of the AGC amp is 2.5 dBm, the feedback path should provide 5 volts back to the AGC control pin. When this occurs, the AGC amplifier will attenuate the signal by 13 dB.

2. Detector Circuit

The purpose of this circuit is to detect when the received and locally produced PN sequences come within half a chip of being in phase. Figure D-5 is a schematic diagram of the threshold detector (U3) used on board 2. When coarse phase alignment is achieved, the signal will de-spread from a wideband signal to a narrowband signal. Once this occurs, the signal power applied to the input of U3 should be sufficient to trigger a detection.



THRESHOLD ADJUST AT +15 VDC BIAS

R_T, Ω	SENSITIVITY dBm (typ)
20	−25
200	−20
2000	−10

Figure D-5 Schematic diagram of the threshold detector (U3) [Ref. 6:p. (5-16)].

Unlike the analog detector this detector does not have to be externally biased, its sensitivity is determined by the value of the resistance seen by the threshold adjust pin. To reduce the possibility of a false detection due to noise, the bandwidth of the BPF should be kept as narrow as possible. However, as the bandwidth goes down, the required Q for the filter goes up. This is why a crystal filter was used. Unfortunately, the crystal filter and its impedance matching circuitry exhibited a higher insertion loss than originally anticipated. The additional insertion loss of the crystal BPF was then compensated for with U13.

Each crystal filter is a two pole BPF with an input and output impedance of 3kΩ and 2pf. To achieve a steeper role off, two crystal filters are cascaded together to create a four pole filter. The input and output must be impedance matched to the source and load, each of which is 50Ω. Since the signal is only 15kHz wide at this point, a narrowband impedance matching circuit is all that is necessary. A narrowband impedance matching circuit has fewer components than the wideband impedance matching circuit and is easier to build. Initial values for the impedance matching circuit were computed using a free CAD program from Hewlett Packard called APPCAD.

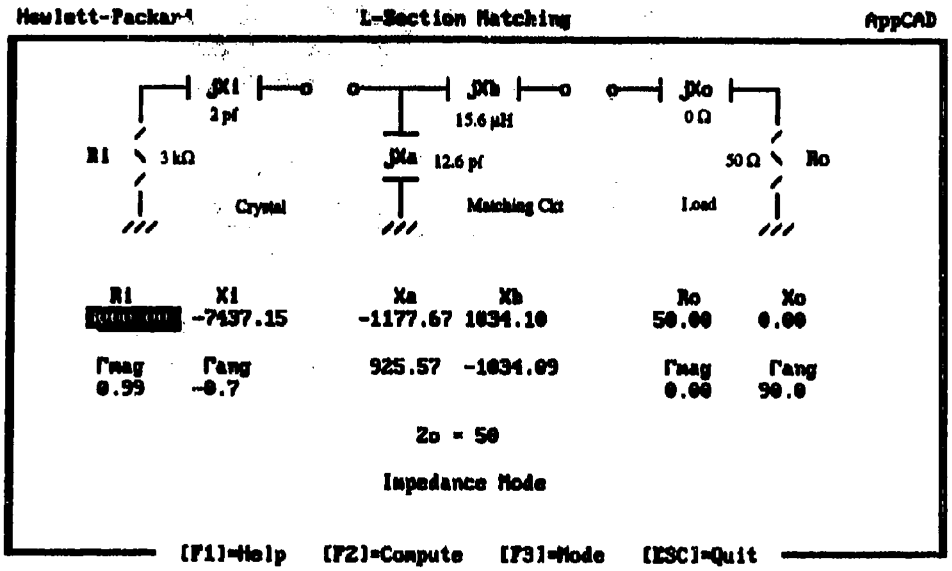


Figure D-6 Snap shot of the monitor screen while using APPCAD to design the impedance matching circuits.

These values were used as a starting point during a crude RF breadboard of the circuit. A variable inductor and variable capacitor were used to determine the best values. As it turned out, the inductor had less of an effect on the circuit than the capacitor. So a variable capacitor will be used in the final bread board to minimize insertion loss of the impedance matching circuit.

C. BOARD 3: PN SEQUENCE TRACKING

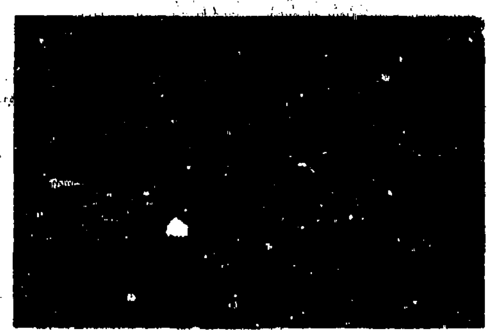


Figure D-7 Partially completed RF bread board of the PN sequence tracking circuit on board 3.

The purpose of this circuit is to provide an error voltage to the VCXO of the locally produced PN sequence generator to allow the locally produced PN sequence to track the phase (or epic) of the received PN sequence. In this design, this is accomplished with an implementation of the non-coherent double dither loop (DDL) [Ref. 5:p. 188-189].

Turning to the schematic of board 3, you may notice a few of the same components and circuits used in the AGC and detector circuit diagrams. This is because each arm of the DDL is very similar to the detector circuit, using the same BPFs and experiencing the same unanticipated additional insertion loss. U1 was placed in the circuit to compensate for these losses and provide a signal of sufficient magnitude for the analog level detectors (U13, U14). These detectors are identical to the one that was used in the AGC feedback circuit. When the received and local PN sequences are aligned, the signal at the input to the analog detectors is expected to be - 6 dBm yielding an output of approximately 200mv. This estimate of the output is based on figure D-8.

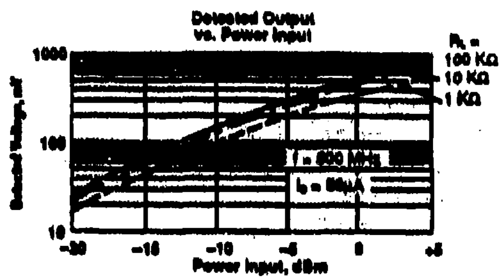


Figure D-8 Graph showing the detected output of the analog detectors vs input power [Ref. 6:p. (5-11)].

The output from each detector, after the reference and detected voltages are summed (U17, U18), then subtracted (U20, U21), to develope and error voltage. The error voltage is amplified (U16) and low pass filtered before it is used to control the 5 MHz HCMOS VCXO on board 6. An indication of lock is developed using a window comparator (U15) which senses when the loop feedback voltage's magnitude exceeds that measured when the loop is tracking. An inverter should be used on board 6 to make this signal a positive voltage when the loop is locked and tracking.

D. BOARD 4: CARRIER TRACKING LOOP AND DEMODULATOR

The purpose of this circuit is to align the phase of the locally produced carrier with that of the received suppressed carrier by producing an error voltage that controls the 10.7 MHz sinewave VCXO on board 5. This is necessary to properly demodulate a BPSK signal, which may only be demodulated coherently. The circuit is an implementation of a Costas loop. This board has not been fabricated because a decision was made to include demodulator circuitry, and that circuitry still remains to be designed. As you can see, some of the circuitry is the same as that used in the previous schematics, and will not be repeated here.

The LPFs that appear in each arm (U9, U10, U12, U13) were implemented using the GIC topology as discussed in Appendix C. The output of each LPF when multiplied together (U14) yields an error signal.

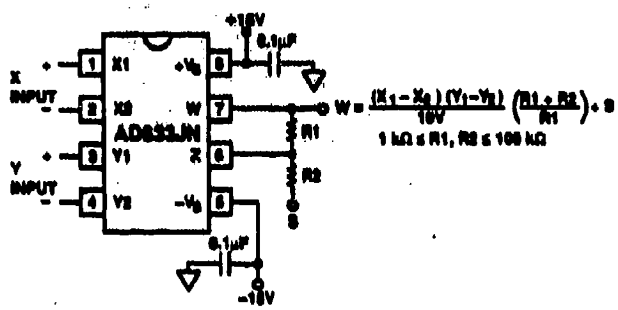


Figure D-9 Four-quadrant analog multiplier used as a phase detector on board 4 [Ref. 13:p. (2-47)].

This error signal represents the phase difference between the two signals, because the two signals are the same frequency and in quadrature. The remaining parts of the circuit such as the amplifier, loop filter, and window comparator are identical to those used on board 3 and discussed in the previous section.

E. BOARD 5: PN PHASE MODULATION AND AMPLIFICATION

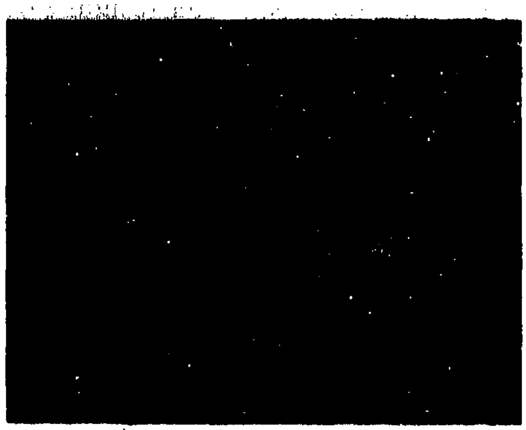


Figure D-10 RF bread board of the PN phase modulation and amplification circuitry on board 5.

The purpose of this circuit is to prepare binary data and PN sequences for mixing. This is accomplished by first bi-phase modulating them on to a carrier, then amplifying the resulting BPSK signal to the level required. Because a number of circuits required bi-phase modulation, it was convenient to place all of them on the same board.

Before arriving on this board the binary data and PN sequences are converted from voltage to current, because the bi-phase modulators (U7, U17, U18, U19, U20) are driven with ± 10 milliampere. This may be done several ways, one of which is shown below

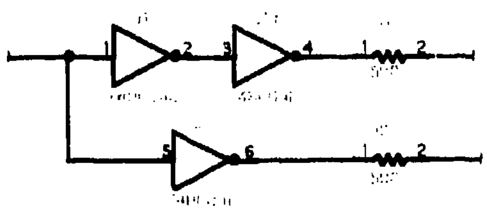


Figure D-11 Circuit used to convert a TTL signal to the ±10ma drive current required by the bi-phase modulators.

To function properly, the carrier power applied to the input of the bi-phase modulators should not exceed -3 dBm. Once functioning, the resulting BPSK signal is then amplified to the level required for mixing on the boards that follow.

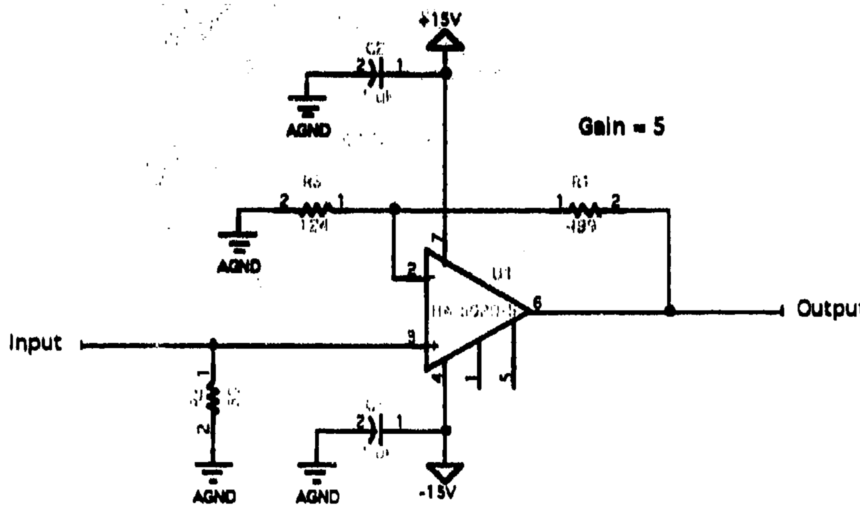


Figure D-12 Typical non-inverting amplifier used on board 5 to amplify a signal to the level required for mixing.

U1 of figure D-9 is a current feedback operational amplifier. A current feedback op-amp was selected because its bandwidth is nearly independent of the closed loop gain. Unlike a voltage feedback amplifiers, whose bandwidth drops rapidly as closed loop gain is increased. This op-amp is very sensitive to the value of R1 as shown in figure D-9.

A_{CL}	Recommended R_F
1	825-1kΩ
2-4	825Ω
5-8	500Ω
9-10	287Ω
20	287Ω

Table D-1: Feedback resistor values recommended by Harris Semiconductor to maintain both bandwidth and stability

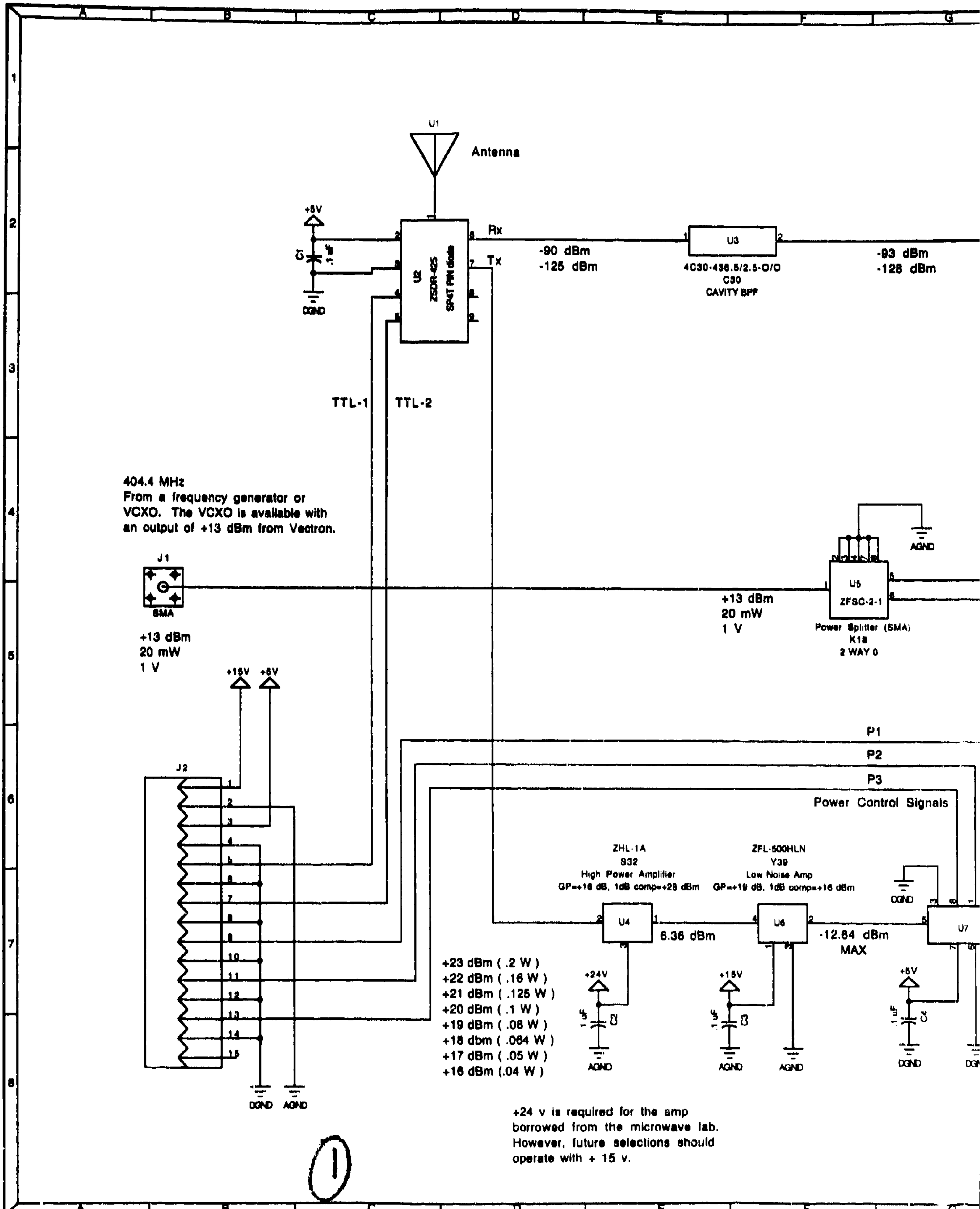
Initial attempts to build this circuit on a crude RF bread board failed, because the value of R_F was too high. After several calls to Harris Semiconductor, the engineer who designed the chip provided the information shown in Table D-1. The amplifier worked great once the proper value of R_F was installed. The fact that a current feedback op-amp is sensitive to the value of the feedback resistor was not obvious at the time, because a voltage feedback amplifier is what is generally discussed in text books.

F. BOARD 6: PN GENERATION AND PHASE SEARCH CIRCUITS

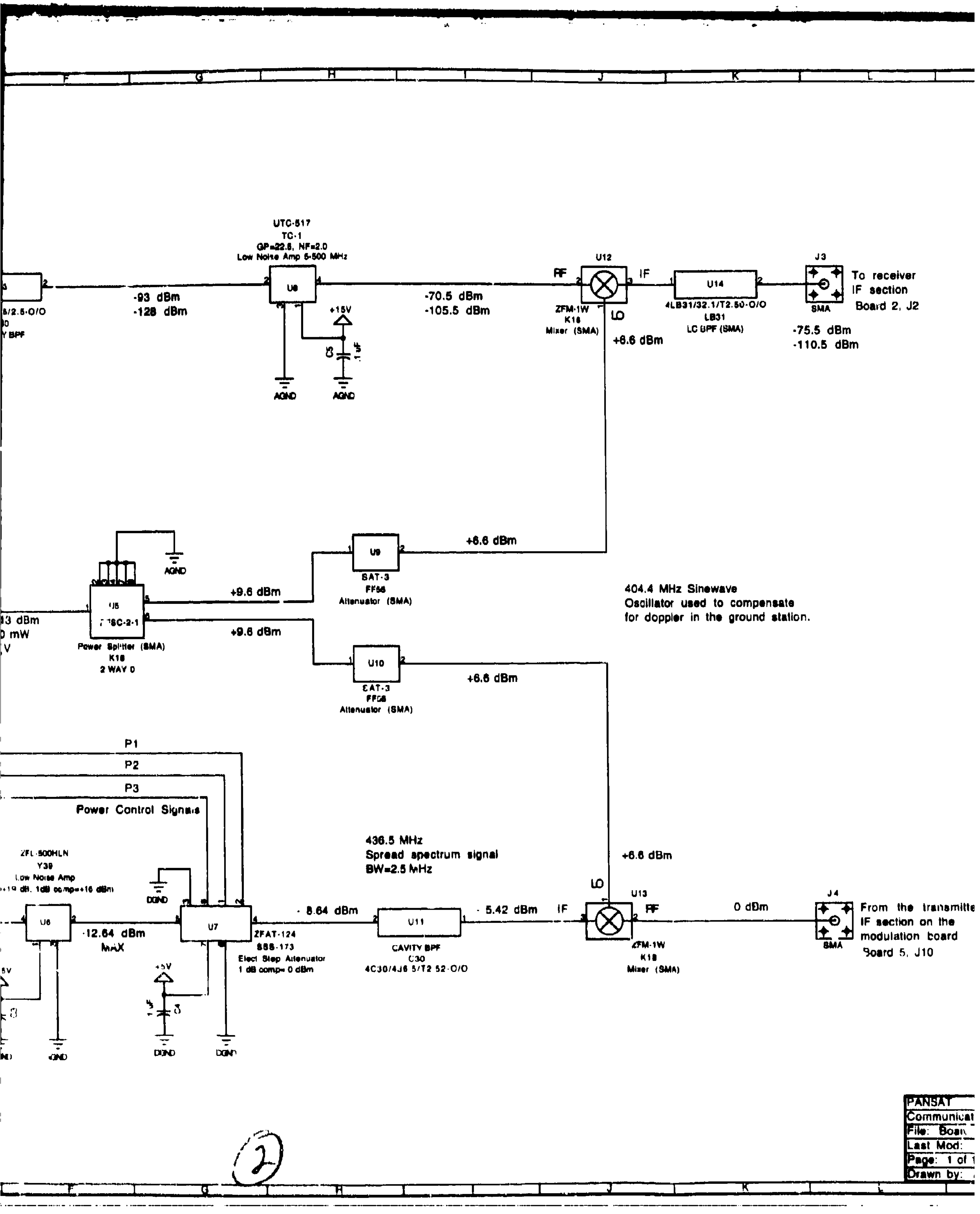
Figure D-13 Digital bread board of the PN phase search circuit shown in the schematic diagram of Board 6.

The purpose of this circuit is to conduct a search for the proper phase of the locally produced PN sequence. Many search strategies have been written about as discussed in chapter three. This design attempts to implement and allow the evaluation of these different search strategies, by allowing the user to program the search strategy to be run. Once the evaluation phase is complete, the desired search strategy may be implemented with a state machine. The state machine would take the place of the computer in the evaluation phase.

This design is completely experimental, and is not based on anything seen or read. Fortunately, because it is digital, it can be easily adapted without having to produce another board, as could occur with the RF bread boards. A detailed discussion of the actual circuit may be fruit less at this point, because the schematic is incomplete.



U1
Antenna
+5V
C1
.1 uF
DGND
U2
ZSDR-425
SP4T PIN diode
Rx
Tx
-90 dBm
-125 dBm
U3
4030-436.5/2.5-O/O
C30
CAVITY BPF
-93 dBm
-128 dBm
TTL-1
TTL-2
404.4 MHz
From a frequency generator or
VCXO. The VCXO is available with
an output of +13 dBm from Vectron.
J1
SMA
+13 dBm
20 mW
1 V
AGND
U5
ZFSC-2-1
Power Splitter (SMA)
K18
2 WAY 0
+15V
+5V
J2
P1
P2
P3
Power Control Signals
ZHL-1A
S32
High Power Amplifier
GP=+16 dB, 1dB comp=+28 dBm
ZFL-500HLN
Y39
Low Noise Amp
GP=+19 dB, 1dB comp=+16 dBm
U4
U6
U7
6.36 dBm
-12.64 dBm
MAX
+23 dBm (.2 W)
+22 dBm (.16 W)
+21 dBm (.125 W)
+20 dBm (.1 W)
+19 dBm (.08 W)
+18 dbm (.064 W)
+17 dBm (.05 W)
+16 dBm (.04 W)
+24V
+15V
+5V
.1 uF
C2
C3
C4
AGND
DGND
+24 v is required for the amp
borrowed from the microwave lab.
However, future selections should
operate with + 15 v.
1


F
G
H
I
J
K
L
UTC-517
TC-1
GP=22.5, NF=2.0
Low Noise Amp 5-500 MHz
U8
-93 dBm
-128 dBm
+15V
AGND
AGND
-70.5 dBm
-105.5 dBm
U12
RF
IF
LO
ZFM-1W
K18
Mixer (SMA)
+6.6 dBm
U14
4LB31/32.1/T2.50-O/O
LB31
LC BPF (SMA)
J3
SMA
To receiver
IF section
Board 2, J2
-75.5 dBm
-110.5 dBm
AGND
U9
SAT-3
FF56
Attenuator (SMA)
+6.6 dBm
+9.6 dBm
+9.6 dBm
U5
Power Splitter (SMA)
K18
2 WAY 0
U10
SAT-3
Attenuator (SMA)
+6.6 dBm
404.4 MHz Sinewave
Oscillator used to compensate
for doppler in the ground station.
P1
P2
P3
Power Control Signals
ZFL-500HLN
Y39
Low Noise Amp
U6
U7
DGND
-12.64 dBm
MAX
ZFAT-124
888-173
Elect Step Attenuator
1 dB comp= 0 dBm
+5V
DGND
DGND
436.5 MHz
Spread spectrum signal
BW=2.5 MHz
-8.64 dBm
U11
CAVITY BPF
C30
4C30/436.5/T2.52-O/O
-5.42 dBm
IF
LO
U13
RF
+6.6 dBm
ZFM-1W
K18
Mixer (SMA)
0 dBm
J4
SMA
From the transmitte
IF section on the
modulation board
Board 5, J10
PANSAT
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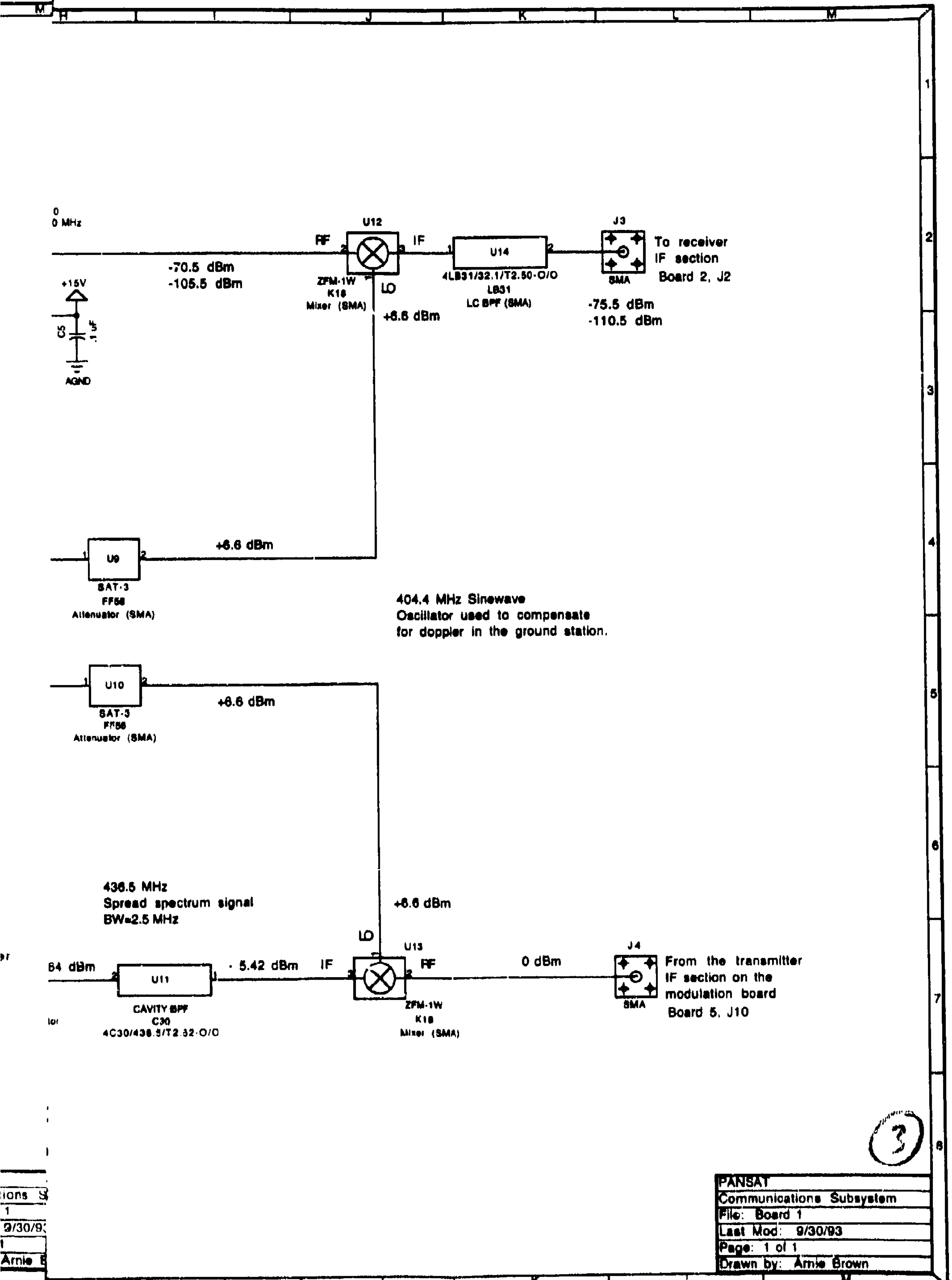
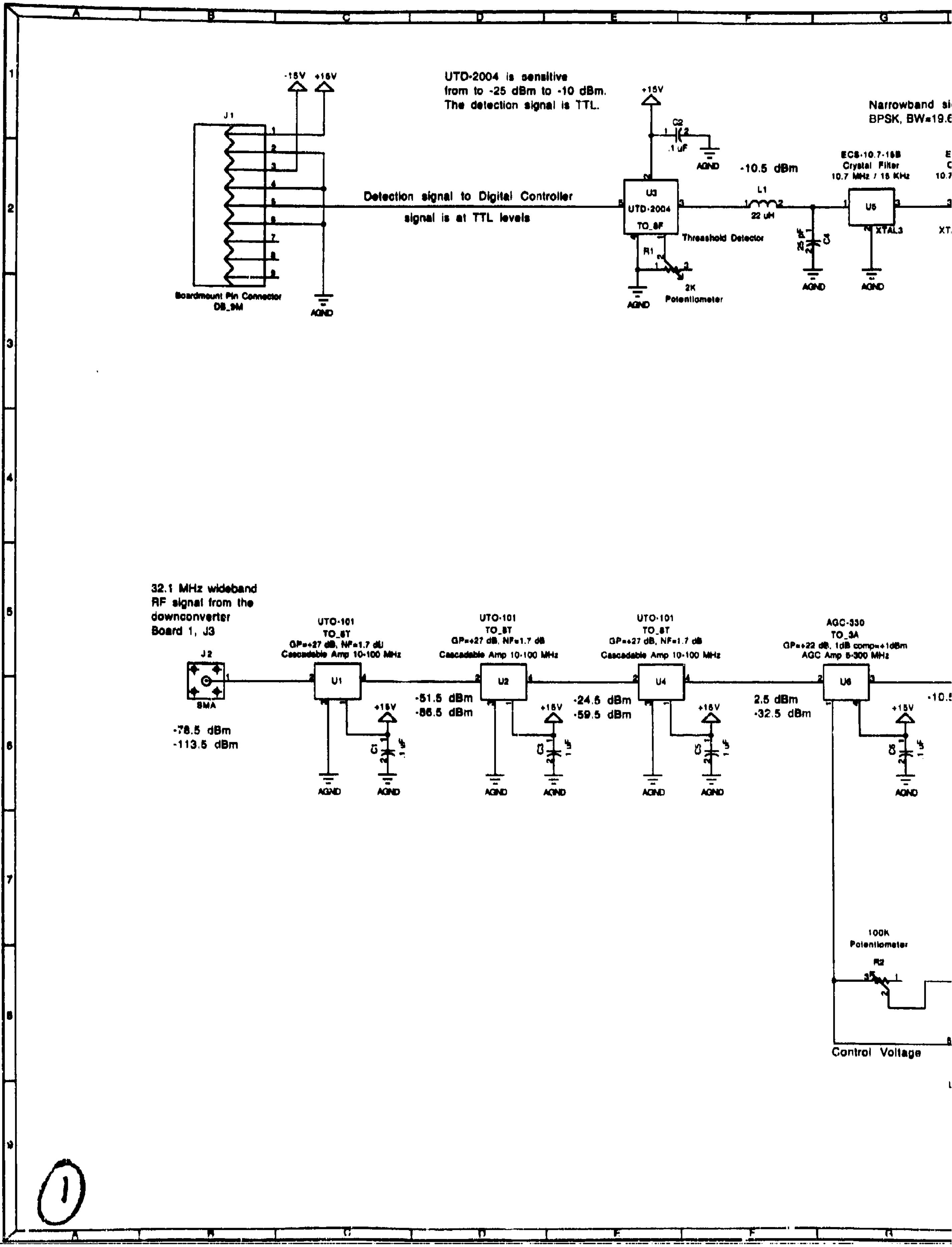
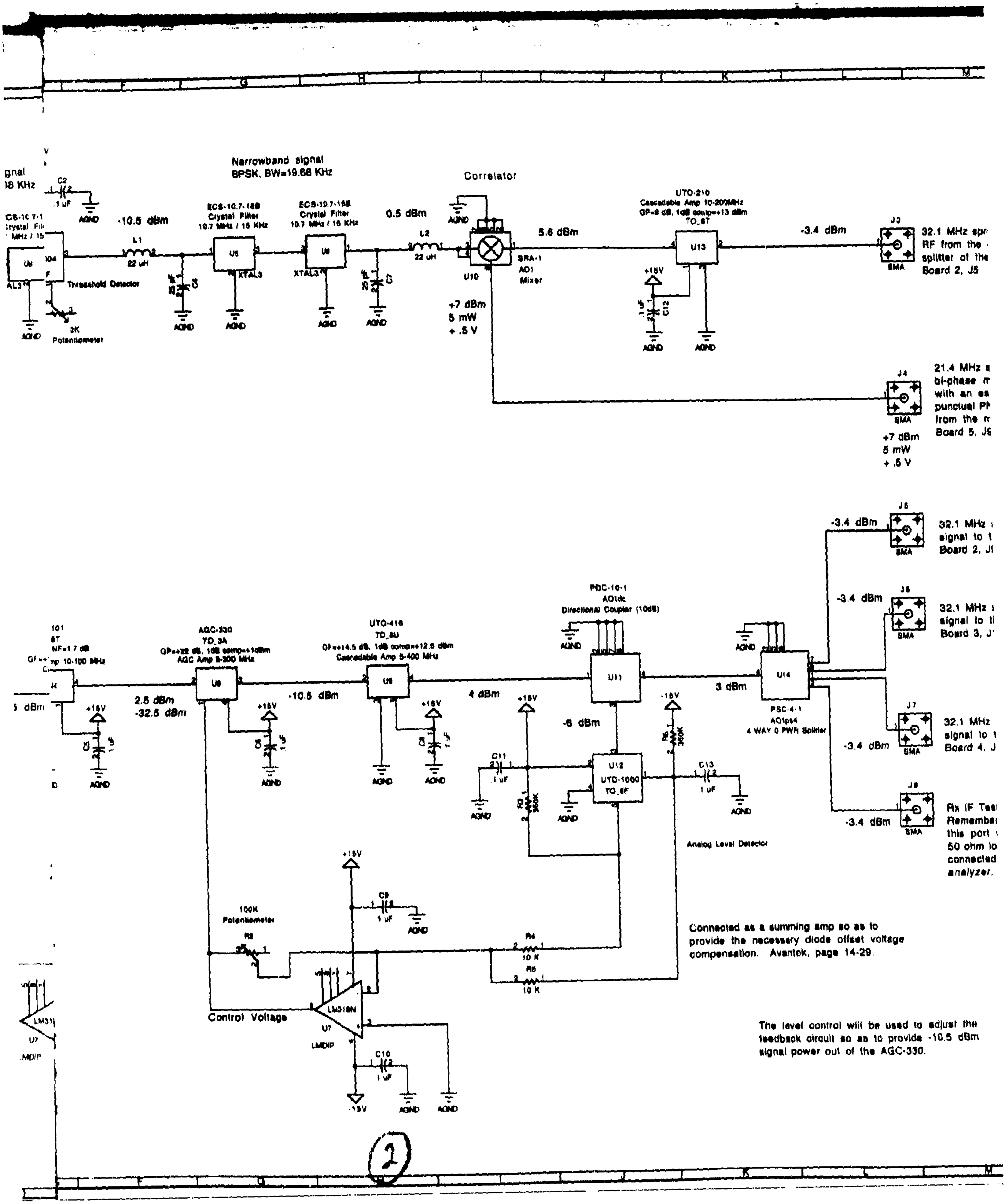
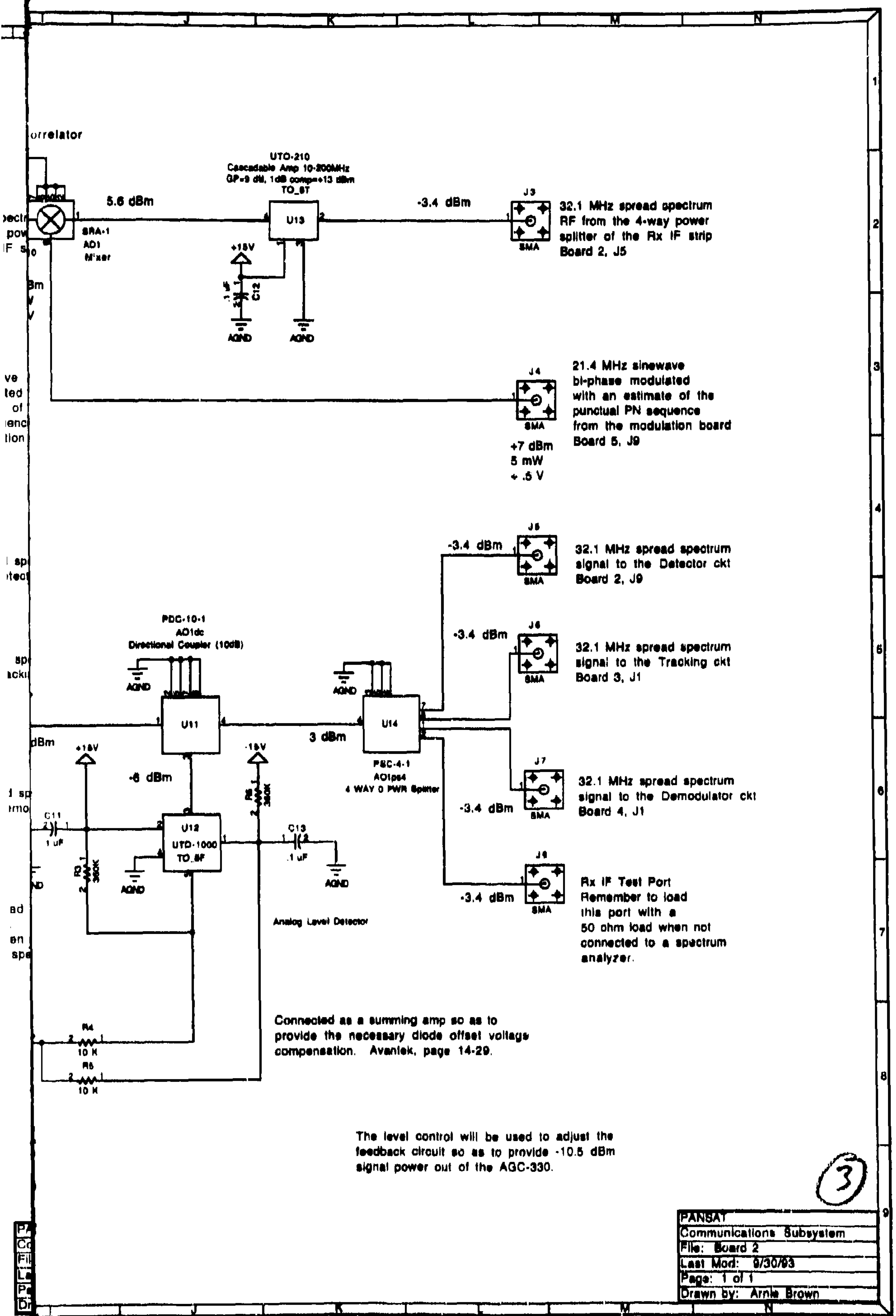
File: Boar
Last Mod:
Page: 1 of
Drawn by:
2


0
0 MHz
U12
RF
IF
U14
J3
To receiver
IF section
Board 2, J2
-70.5 dBm
-105.5 dBm
+15V
C5
.1 uF
AGND
ZFM-1W
K18
Mixer (SMA)
LO
+6.6 dBm
4LB31/32.1/T2.50-O/O
LB31
LC BPF (SMA)
SMA
-75.5 dBm
-110.5 dBm
U9
+6.6 dBm
SAT-3
FF56
Attenuator (SMA)
404.4 MHz Sinewave
Oscillator used to compensate
for doppler in the ground station.
U10
+6.6 dBm
SAT-3
FF56
Attenuator (SMA)
436.5 MHz
Spread spectrum signal
BW=2.5 MHz
+6.6 dBm
LO
U13
J4
64 dBm
U11
- 5.42 dBm
IF
RF
0 dBm
From the transmitter
IF section on the
modulation board
Board 5, J10
CAVITY BPF
C30
4C30/436.5/T2.32-O/O
ZFM-1W
K18
Mixer (SMA)
SMA
3
PANSAT
Communications Subsystem
File: Board 1
Last Mod: 9/30/93
Page: 1 of 1
Drawn by: Arnie Brown


UTD-2004 is sensitive
from to -25 dBm to -10 dBm.
The detection signal is TTL.
-15V +15V
J1
Boardmount Pin Connector
DB_9M
AGND
Detection signal to Digital Controller
signal is at TTL levels
+15V
C2
.1 uF
U3
UTD-2004
TO_8F
Threshold Detector
R1
2K
Potentiometer
-10.5 dBm
L1
22 uH
C4
ECS-10.7-15B
Crystal Filter
10.7 MHz / 15 KHz
U5
XTAL3
Narrowband si
BPSK, BW=19.6
32.1 MHz wideband
RF signal from the
downconverter
Board 1, J3
J2
SMA
-78.5 dBm
-113.5 dBm
UTO-101
TO_8T
GP=+27 dB, NF=1.7 dB
Cascadable Amp 10-100 MHz
U1
-51.5 dBm
-86.5 dBm
U2
-24.5 dBm
-59.5 dBm
U4
2.5 dBm
-32.5 dBm
AGC-330
TO_3A
GP=+22 dB, 1dB comp=+1dBm
AGC Amp 5-300 MHz
U6
-10.5
C1
C3
C5
C6
.1 uF
100K
Potentiometer
R2
Control Voltage
1



Narrowband signal
BPSK, BW=19.68 KHz
Correlator
-10.5 dBm
ECS-10.7-15B Crystal Filter 10.7 MHz / 15 KHz
0.5 dBm
5.6 dBm
UTO-210 Cascadable Amp 10-200MHz
TO_8T
-3.4 dBm
32.1 MHz
RF from the
splitter of the
Board 2, J5
Threshold Detector
2K Potentiometer
SRA-1
AO1
Mixer
+7 dBm
5 mW
+ .5 V
21.4 MHz
bi-phase
with an
punctual
from the
Board 5,
AGC-330
TO_3A
AGC Amp 5-300 MHz
UTO-416
TO_8U
Cascadable Amp 5-400 MHz
PDC-10-1
AO1dc
Directional Coupler (10dB)
2.5 dBm
-32.5 dBm
-10.5 dBm
4 dBm
3 dBm
-6 dBm
PSC-4-1
AO1ps4
4 WAY 0 PWR Splitter
UTO-1000
TO_8F
Analog Level Detector
Rx IF Test
Remember
this port
50 ohm
connected
analyzer.
100K Potentiometer
Control Voltage
LM318N
LMDIP
Connected as a summing amp so as to provide the necessary diode offset voltage compensation. Avantek, page 14-29.
The level control will be used to adjust the feedback circuit so as to provide -10.5 dBm signal power out of the AGC-330.



orrelator
UTO-210
Cascadable Amp 10-200MHz
5.6 dBm
-3.4 dBm
U13
SRA-1
AD1
Mixer
+15V
C12
AGND
J3
SMA
32.1 MHz spread spectrum RF from the 4-way power splitter of the Rx IF strip Board 2, J5
J4
SMA
21.4 MHz sinewave bi-phase modulated with an estimate of the punctual PN sequence from the modulation board Board 5, J9
+7 dBm
5 mW
+ .5 V
J5
-3.4 dBm
32.1 MHz spread spectrum signal to the Detector ckt Board 2, J9
PDC-10-1
AD1dc
Directional Coupler (10dB)
J6
-3.4 dBm
32.1 MHz spread spectrum signal to the Tracking ckt Board 3, J1
U11
U14
3 dBm
+15V
-15V
-6 dBm
PSC-4-1
AD1ps4
4 WAY 0 PWR Splitter
J7
-3.4 dBm
32.1 MHz spread spectrum signal to the Demodulator ckt Board 4, J1
C11
1 uF
U12
UTO-1000
TO_8F
C13
.1 uF
R6
360K
R3
360K
AGND
J8
-3.4 dBm
Rx IF Test Port Remember to load this port with a 50 ohm load when not connected to a spectrum analyzer.
Analog Level Detector
R4
10 K
R5
10 K
Connected as a summing amp so as to provide the necessary diode offset voltage compensation. Avantek, page 14-29.
The level control will be used to adjust the feedback circuit so as to provide -10.5 dBm signal power out of the AGC-330.
3
PANSAT
Communications Subsystem
File: Board 2
Last Mod: 9/30/93
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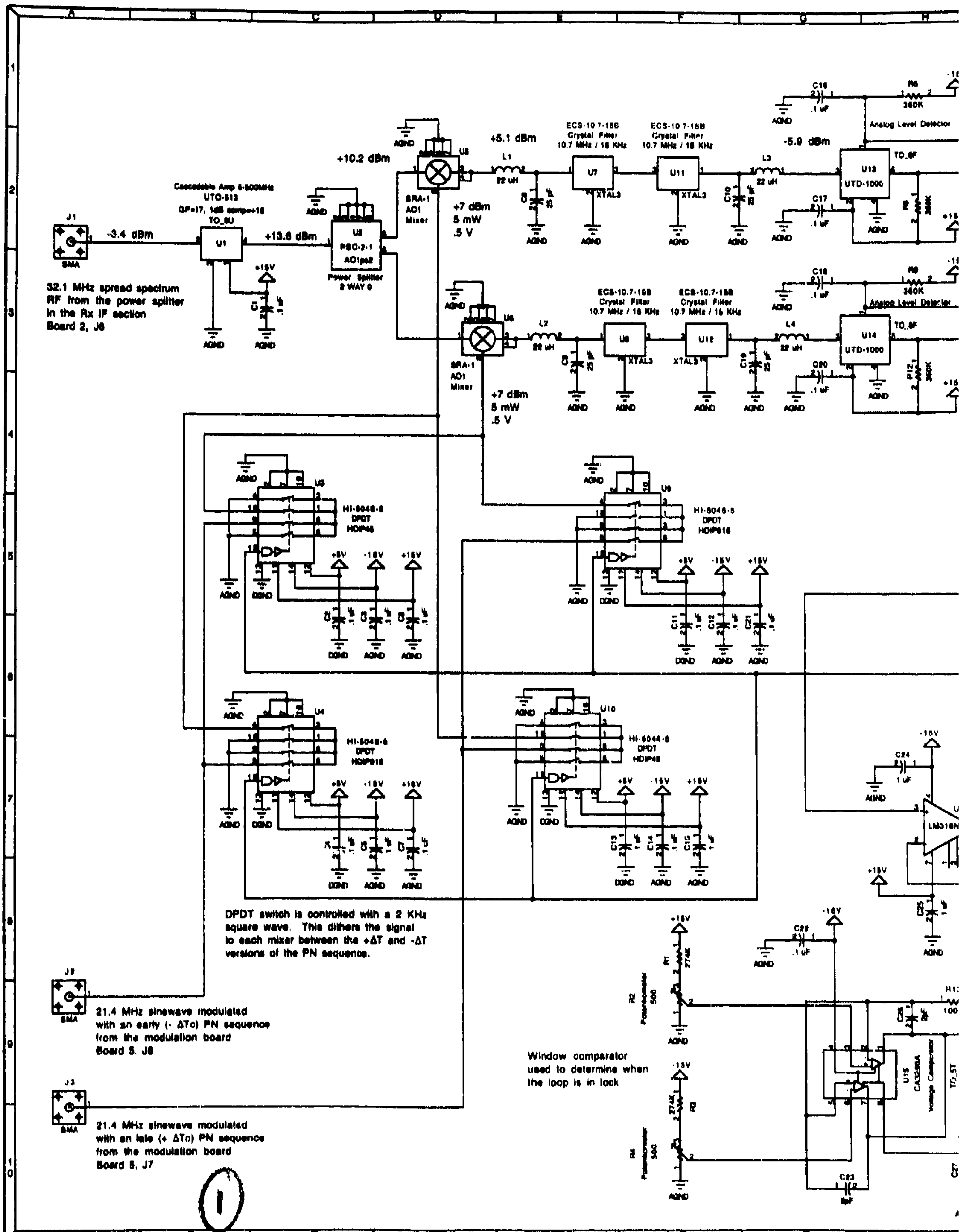
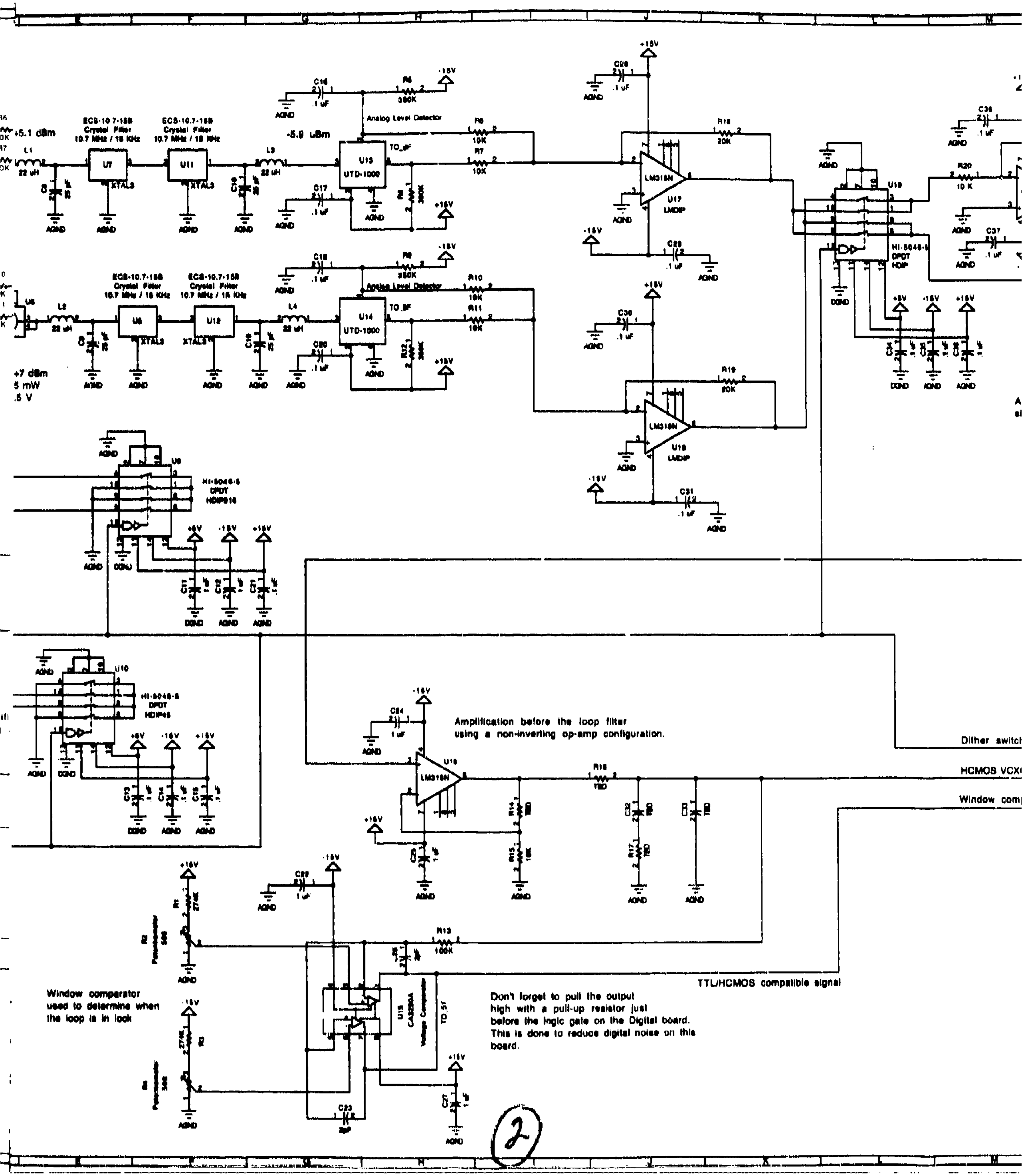
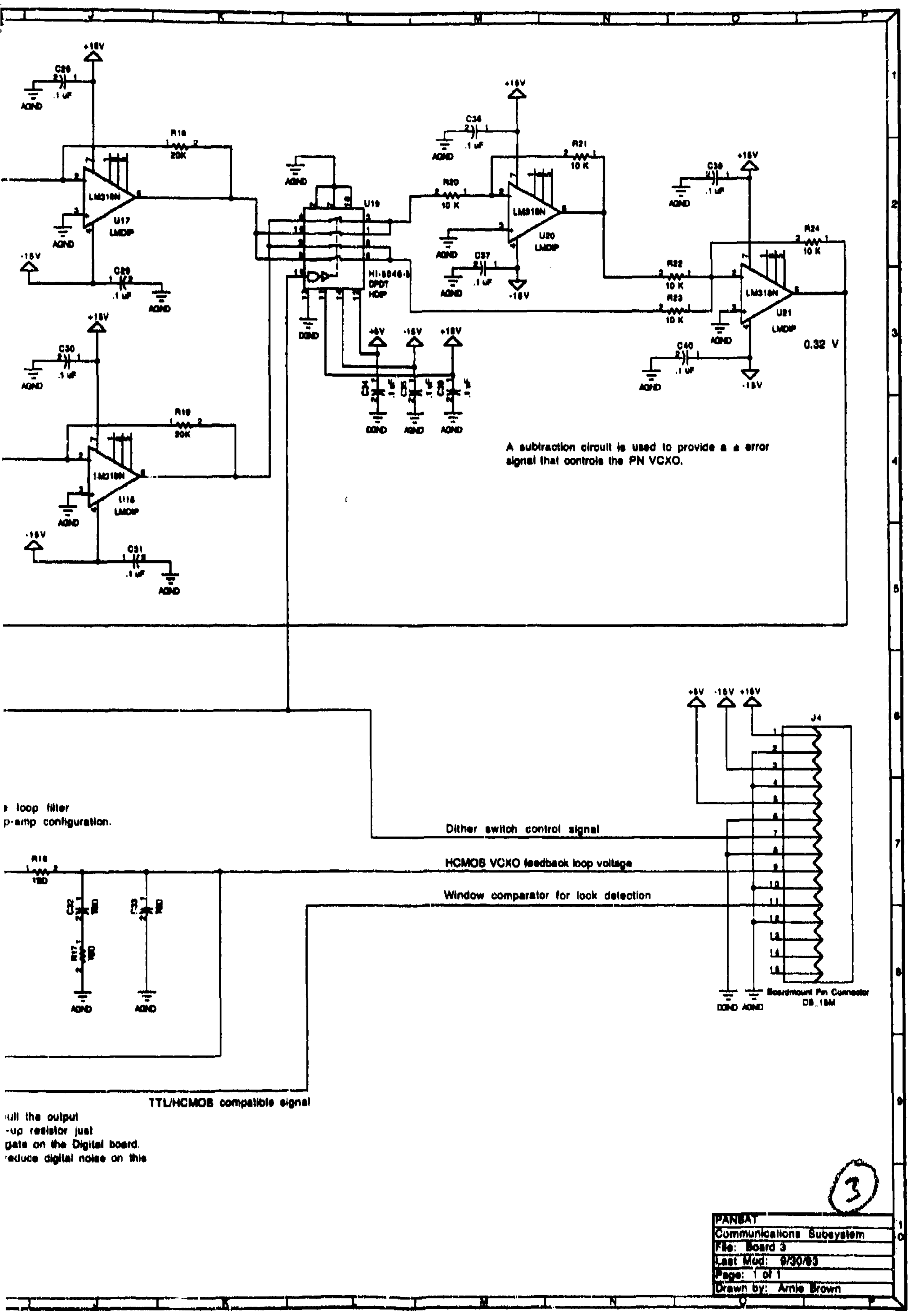
Drawn by: Arnie Brown



32.1 MHz spread spectrum RF from the power splitter in the Rx IF section Board 2, J6
Cascadable Amp 5-500MHz UTO-513
+10.2 dBm
+5.1 dBm
-5.9 dBm
ECS-10.7-15B Crystal Filter 10.7 MHz / 15 KHz
Analog Level Detector
UTD-1000
SRA-1 AO1 Mixer
+7 dBm 5 mW .5 V
PSC-2-1 Power Splitter 2 WAY 0
-3.4 dBm
+13.6 dBm
HI-5046-5 DPDT
LM318N
DPDT switch is controlled with a 2 KHz square wave. This dithers the signal to each mixer between the +ΔT and -ΔT versions of the PN sequence.
21.4 MHz sinewave modulated with an early (- ΔTc) PN sequence from the modulation board Board 5, J6
21.4 MHz sinewave modulated with an late (+ ΔTc) PN sequence from the modulation board Board 5, J7
Window comparator used to determine when the loop is in lock
CA339A Voltage Comparator



+5.1 dBm
ECS-10.7-15B Crystal Filter 10.7 MHz / 15 KHz
-5.9 dBm
Analog Level Detector
UTD-1000
LM318N
LMDIP
HI-5046-5 DPDT HDIP
+7 dBm
5 mW
.5 V
HDIP816
HDIP45
Amplification before the loop filter using a non-inverting op-amp configuration.
Dither switch
HCMOS VCX
Window com
TTL/HCMOS compatible signal
Window comparator used to determine when the loop is in lock
CA3290A Voltage Comparator
Don't forget to pull the output high with a pull-up resistor just before the logic gate on the Digital board. This is done to reduce digital noise on this board.
2



A subtraction circuit is used to provide a a error signal that controls the PN VCXO.
0.32 V
loop filter
p-amp configuration.
Dither switch control signal
HCMOS VCXO feedback loop voltage
Window comparator for lock detection
TTL/HCMOS compatible signal
ull the output
-up resistor just
gate on the Digital board.
educe digital noise on this
Boardmount Pin Connector
DB_15M
J4
U17
U18
U19
U20
U21
LM318N
LMDIP
HI-5046-5
DPDT
HDIP
R18
R19
R20
R21
R22
R23
R24
20K
10 K
AGND
DGND
+15V
-15V
+5V
PANSAT
Communications Subsystem
File: Board 3
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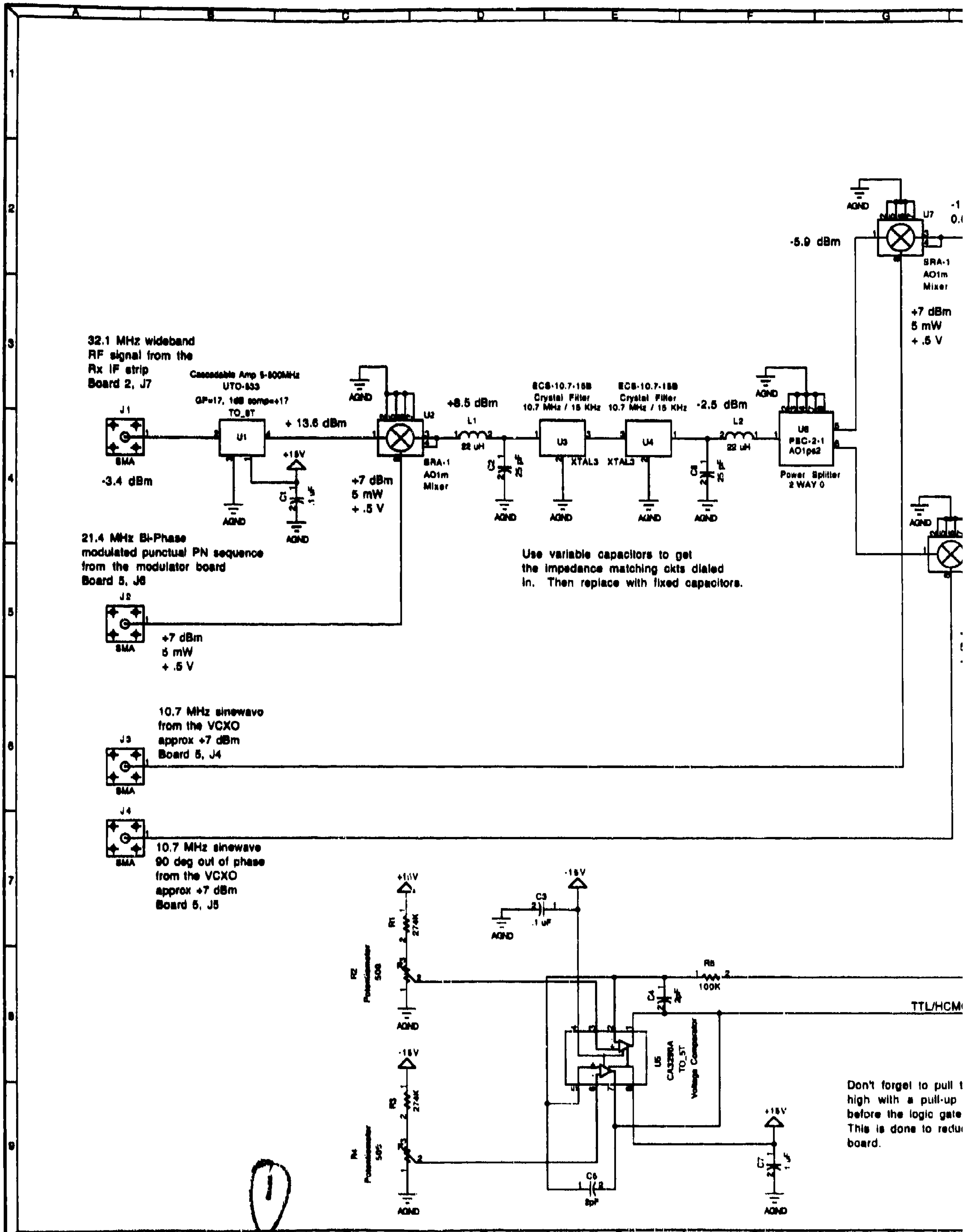
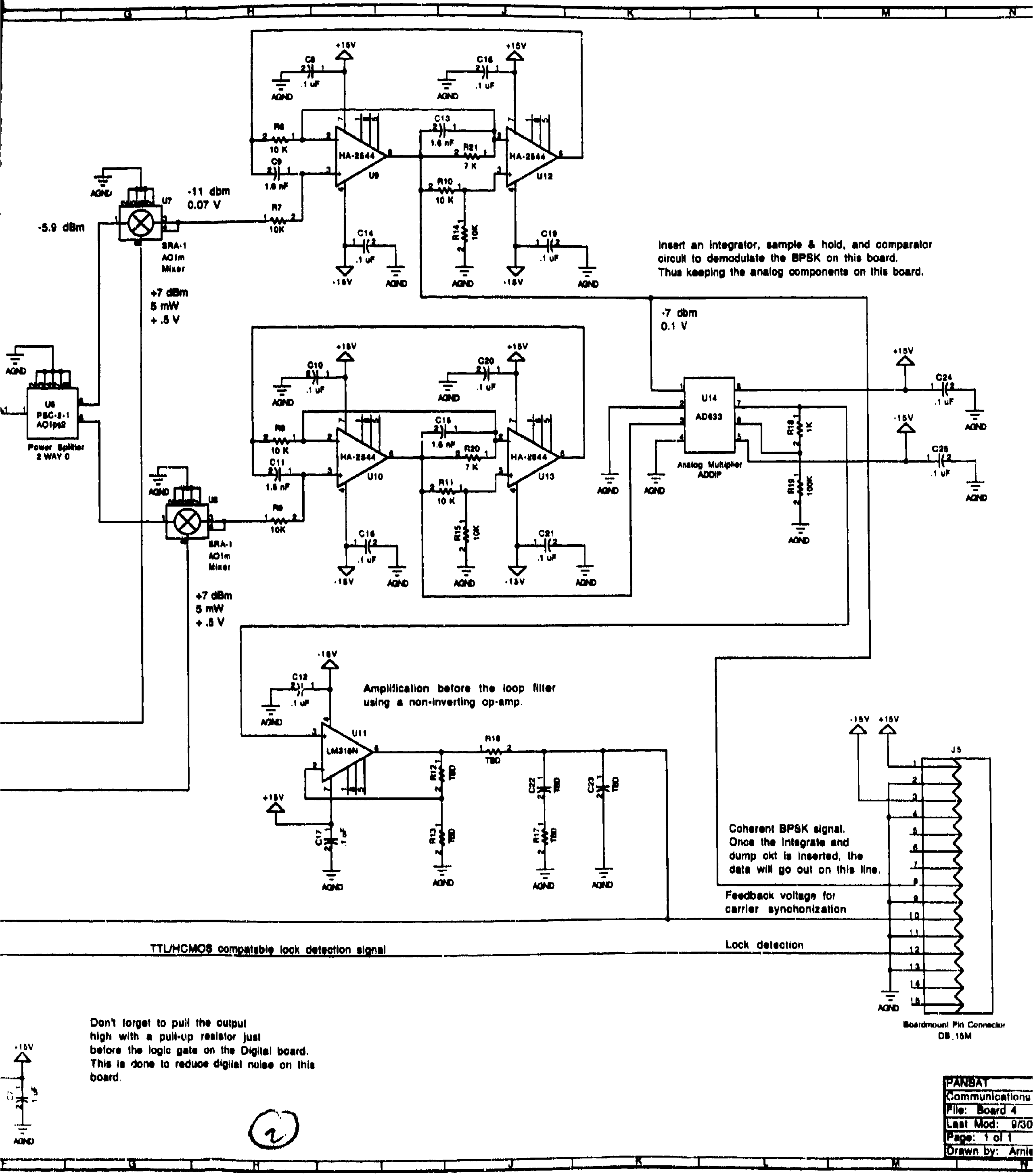
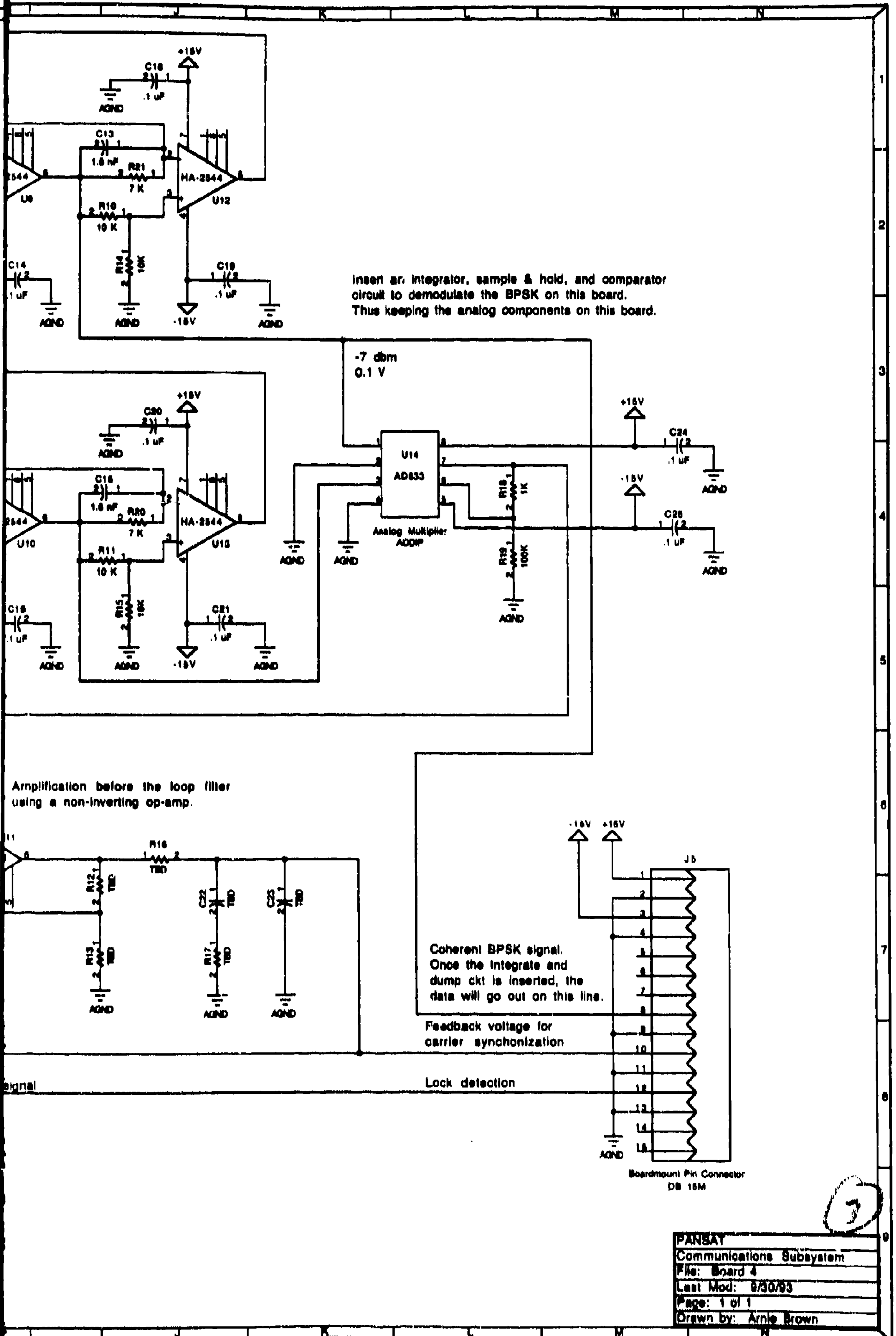
3



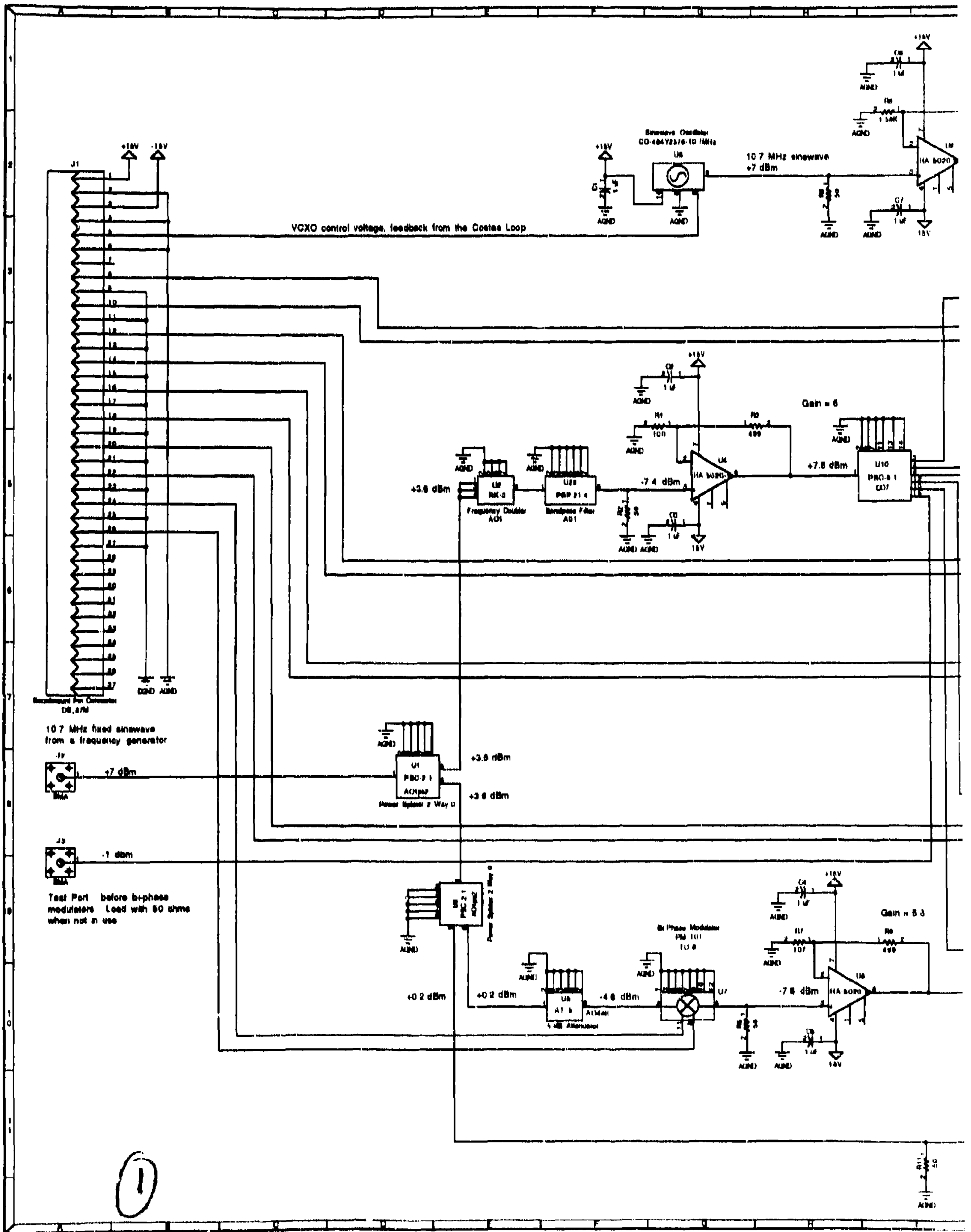
32.1 MHz wideband RF signal from the Rx IF strip Board 2, J7
J1
SMA
-3.4 dBm
Cascadable Amp 5-500MHz
UTO-533
TO_8T
U1
+ 13.6 dBm
+15V
.1 uF
AGND
U2
SRA-1
AO1m
Mixer
+7 dBm
5 mW
+.5 V
+8.5 dBm
L1
22 uH
ECS-10.7-15B
Crystal Filter
10.7 MHz / 15 KHz
U3
U4
XTAL3
-2.5 dBm
L2
22 uH
U6
PSC-2-1
AO1ps2
Power Splitter
2 WAY 0
-5.9 dBm
U7
SRA-1
AO1m
Mixer
+7 dBm
5 mW
+.5 V
21.4 MHz Bi-Phase modulated punctual PN sequence from the modulator board Board 5, J6
J2
SMA
+7 dBm
5 mW
+.5 V
Use variable capacitors to get the impedance matching ckts dialed in. Then replace with fixed capacitors.
10.7 MHz sinewave from the VCXO approx +7 dBm Board 5, J4
J3
SMA
J4
SMA
10.7 MHz sinewave 90 deg out of phase from the VCXO approx +7 dBm Board 5, J5
+15V
R1
274K
R2
Potentiometer
-15V
C3
.1 uF
AGND
R5
100K
C4
TTL/HCM
U5
CA3290A
TO_5T
Voltage Comparator
-15V
R3
274K
R4
Potentiometer
C5
5pF
+15V
C7
.1 uF
Don't forget to pull high with a pull-up before the logic gate This is done to redu board.
A
B
C
D
E
F
G
1
2
3
4
5
6
7
8
9



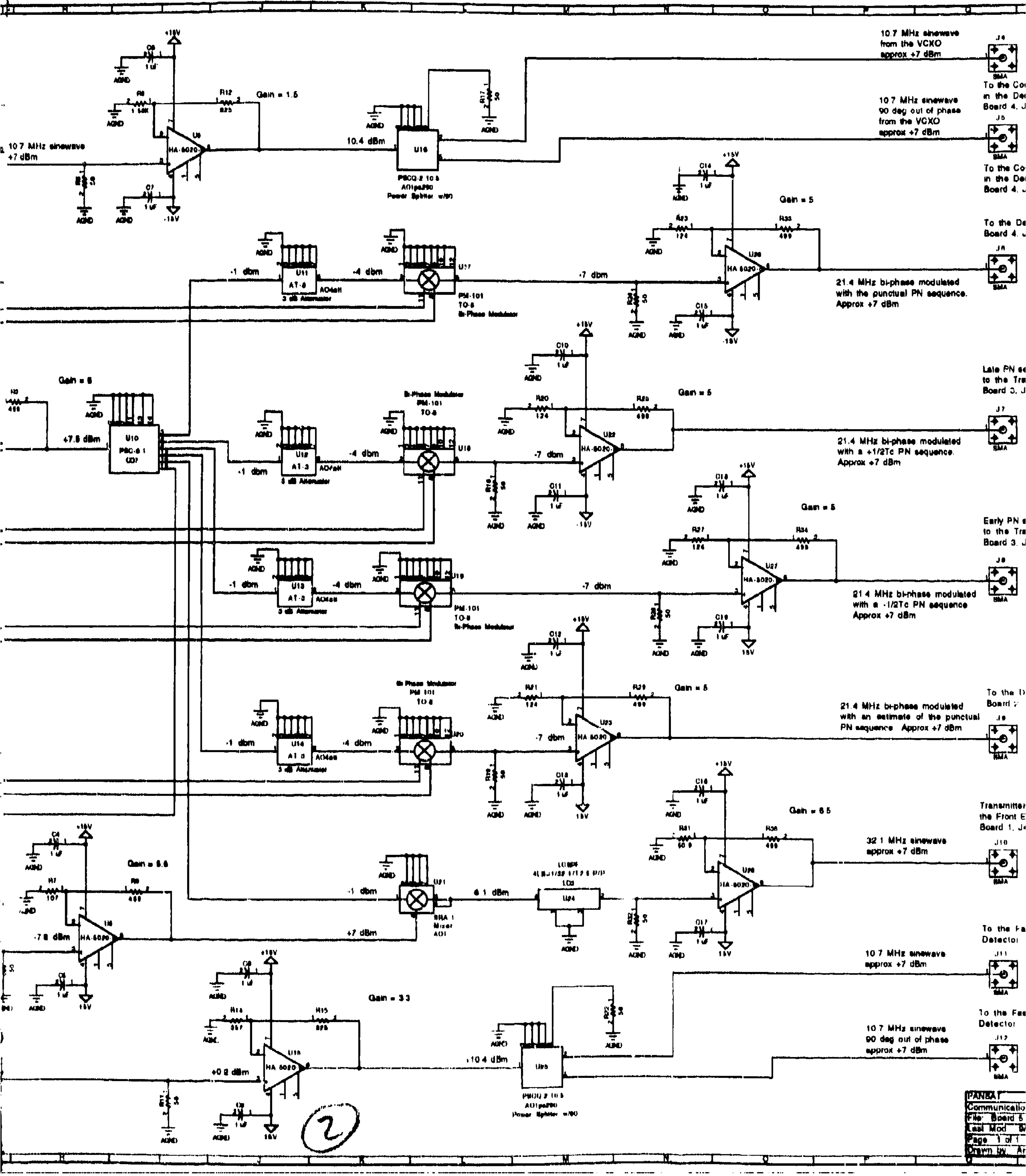
-11 dbm
0.07 V
-5.9 dBm
SRA-1
AO1m
Mixer
+7 dBm
5 mW
+.5 V
U6
PSC-2-1
AO1ps2
Power Splitter
2 WAY 0
HA-2544
U9
U12
U10
U13
-7 dbm
0.1 V
U14
AD633
Analog Multiplier
ADDIP
Insert an integrator, sample & hold, and comparator circuit to demodulate the BPSK on this board. Thus keeping the analog components on this board.
Amplification before the loop filter using a non-inverting op-amp.
U11
LM318N
Coherent BPSK signal. Once the integrate and dump ckt is inserted, the data will go out on this line.
Feedback voltage for carrier synchonization
Lock detection
TTL/HCMOS compatable lock detection signal
J5
Boardmount Pin Connector
DB_15M
Don't forget to pull the output high with a pull-up resistor just before the logic gate on the Digital board. This is done to reduce digital noise on this board.
PANSAT
Communications
File: Board 4
Last Mod: 9/30
Page: 1 of 1
Drawn by: Arnie



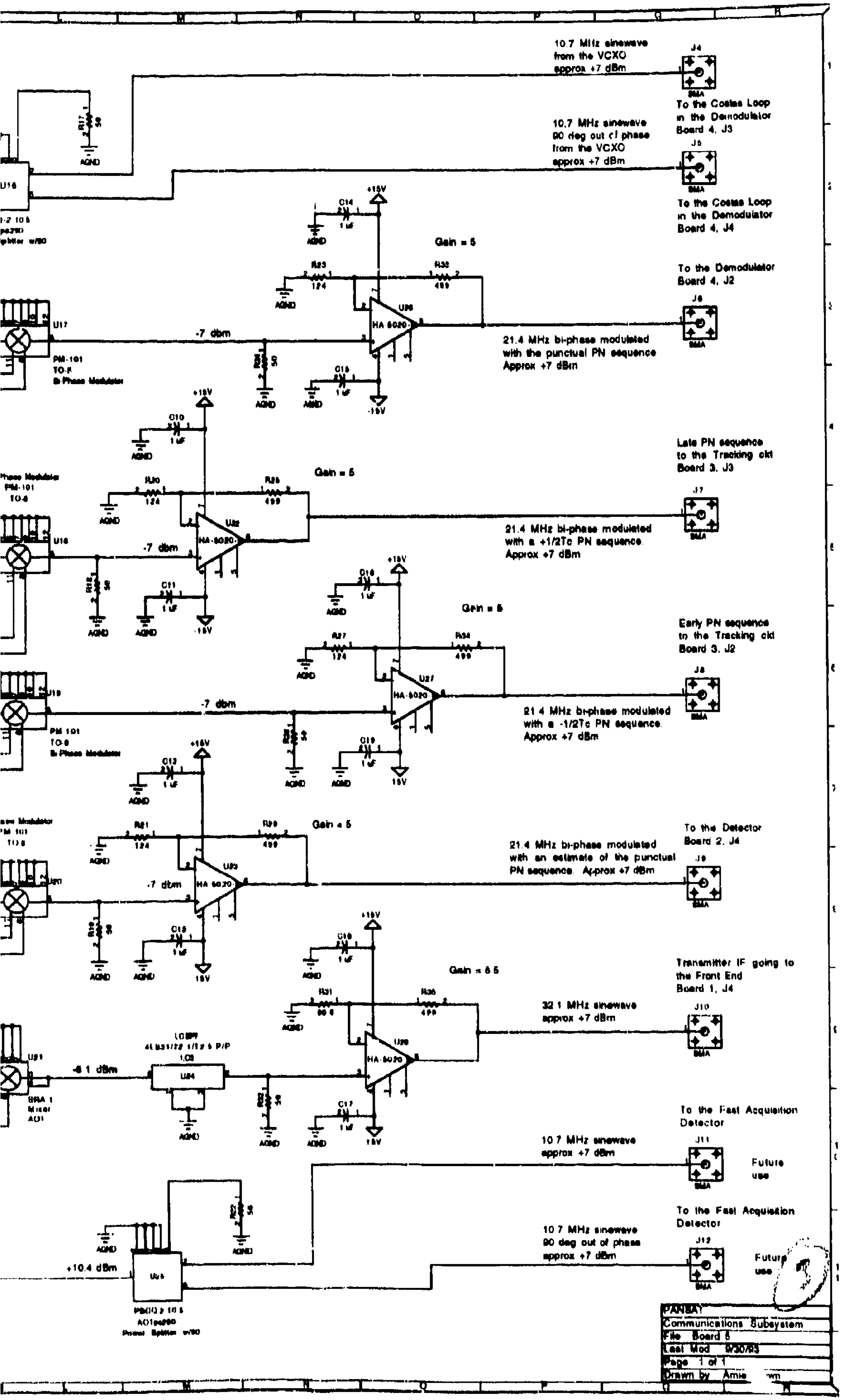
Insert an integrator, sample & hold, and comparator circuit to demodulate the BPSK on this board.
Thus keeping the analog components on this board.
-7 dbm
0.1 V
+15V
-15V
AGND
C18
C13
C14
C19
C20
C16
C18
C21
C24
C25
.1 uF
1.8 nF
R21
R20
7 K
R10
R11
10 K
R14
R15
10K
HA-2544
U9
U10
U11
U12
U13
U14
AD633
Analog Multiplier
ADDIP
R18
1K
R19
100K
Amplification before the loop filter
using a non-inverting op-amp.
R16
R12
R13
R17
C22
C23
TBD
J5
Coherent BPSK signal.
Once the integrate and
dump ckt is inserted, the
data will go out on this line.
Feedback voltage for
carrier synchonization
Lock detection
signal
Boardmount Pin Connector
DB 15M
PANSAT
Communications Subsystem
File: Board 4
Last Mod: 9/30/93
Page: 1 of 1
Drawn by: Arnie Brown

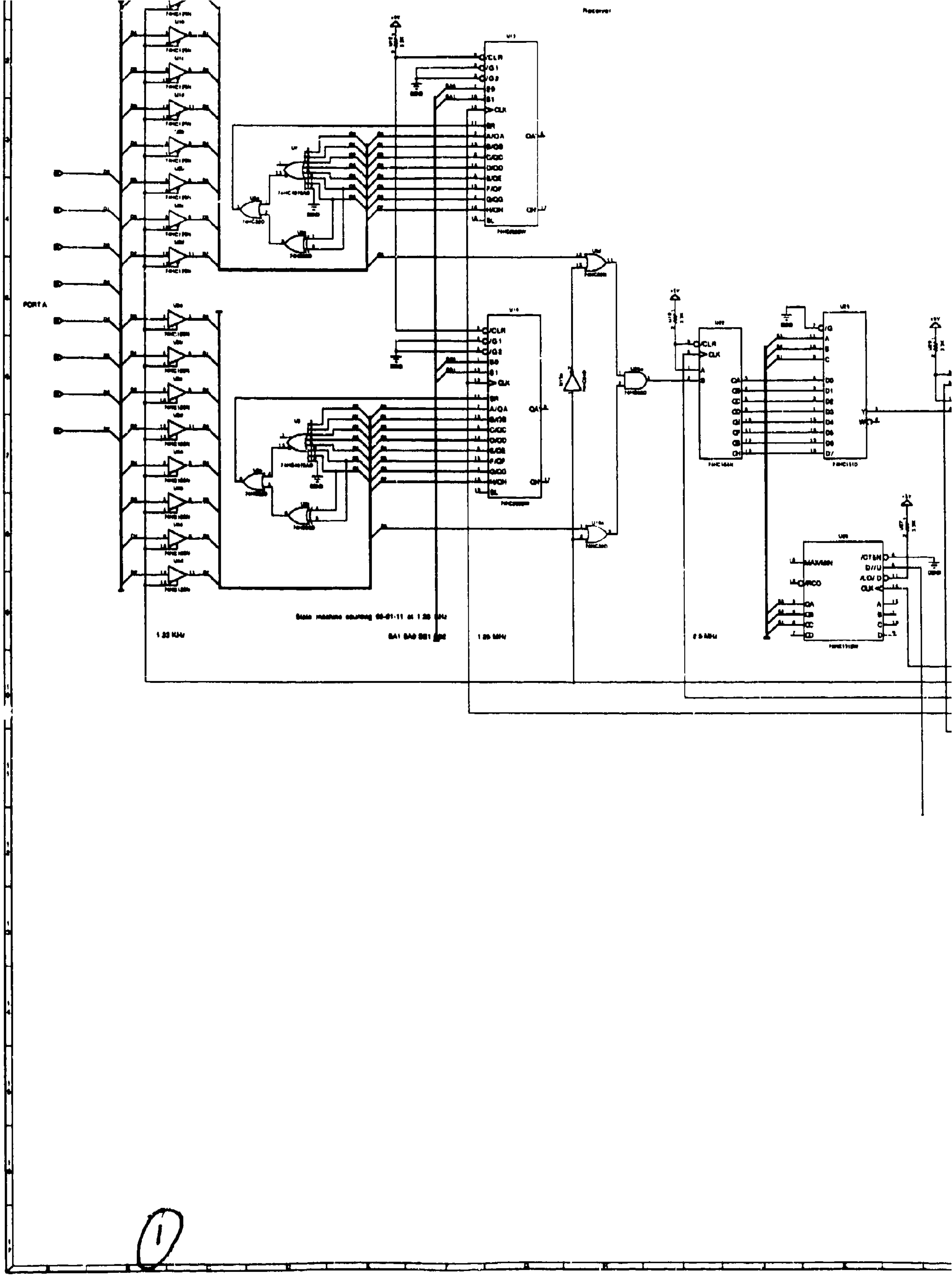


VCXO control voltage, feedback from the Costas Loop
10 7 MHz sinewave
+7 dBm
Gain = 5
+7.6 dBm
+3.6 dBm
-7 4 dBm
Frequency Doubler
Bandpass Filter
10 7 MHz fixed sinewave
from a frequency generator
+7 dBm
+3.6 dBm
+3 6 dBm
-1 dbm
Test Port before bi-phase
modulators Load with 50 ohms
when not in use
+0 2 dBm
+0 2 dBm
-4 6 dBm
-7 8 dBm
DGND
AGND
1

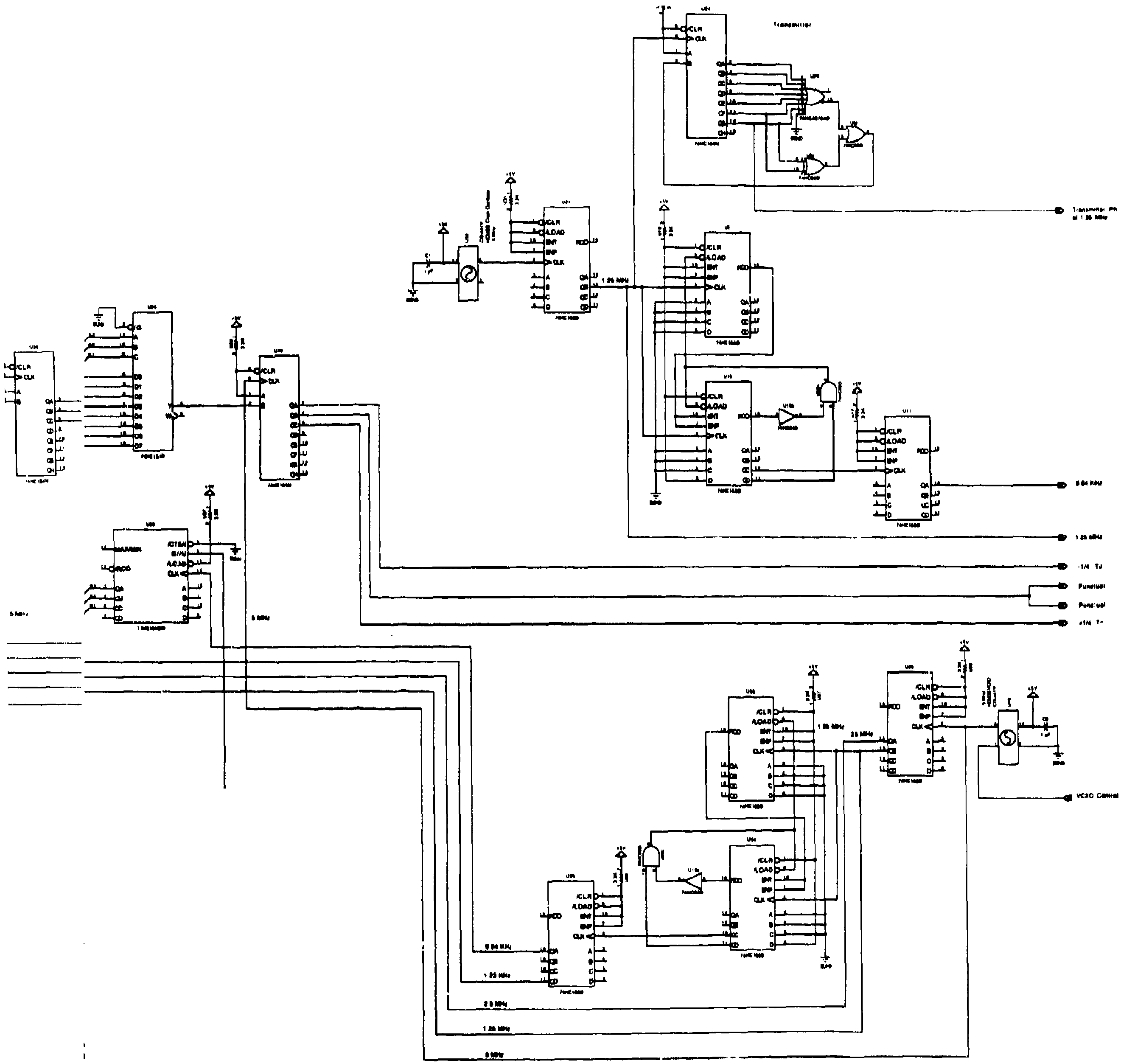


10.7 MHz sinewave from the VCXO approx +7 dBm
10.7 MHz sinewave 90 deg out of phase from the VCXO approx +7 dBm
10.7 MHz sinewave +7 dBm
Gain = 1.5
10.4 dBm
PSCQ-2-10.5
Power Splitter w/90
Gain = 5
-1 dbm
-4 dbm
-7 dbm
AT-3
3 dB Attenuator
PM-101
TO-8
Bi-Phase Modulator
21.4 MHz bi-phase modulated with the punctual PN sequence. Approx +7 dBm
Gain = 6
+7.8 dBm
PSC-6-1
21.4 MHz bi-phase modulated with a +1/2Tc PN sequence. Approx +7 dBm
21.4 MHz bi-phase modulated with a -1/2Tc PN sequence Approx +7 dBm
21.4 MHz bi-phase modulated with an estimate of the punctual PN sequence Approx +7 dBm
Gain = 6.5
32.1 MHz sinewave approx +7 dBm
Gain = 5.5
-7.8 dBm
+7 dBm
6.1 dBm
SRA-1
Mixer
10.7 MHz sinewave approx +7 dBm
10.7 MHz sinewave 90 deg out of phase approx +7 dBm
Gain = 3.3
+0.2 dBm
+10.4 dBm
HA-5020
+15V
-15V
AGND
SMA
Late PN
Early PN
To the Fast Detector
Transmitter
PANSAT
Communication
File: Board 5
Last Mod
Page 1 of 1
Drawn by
2

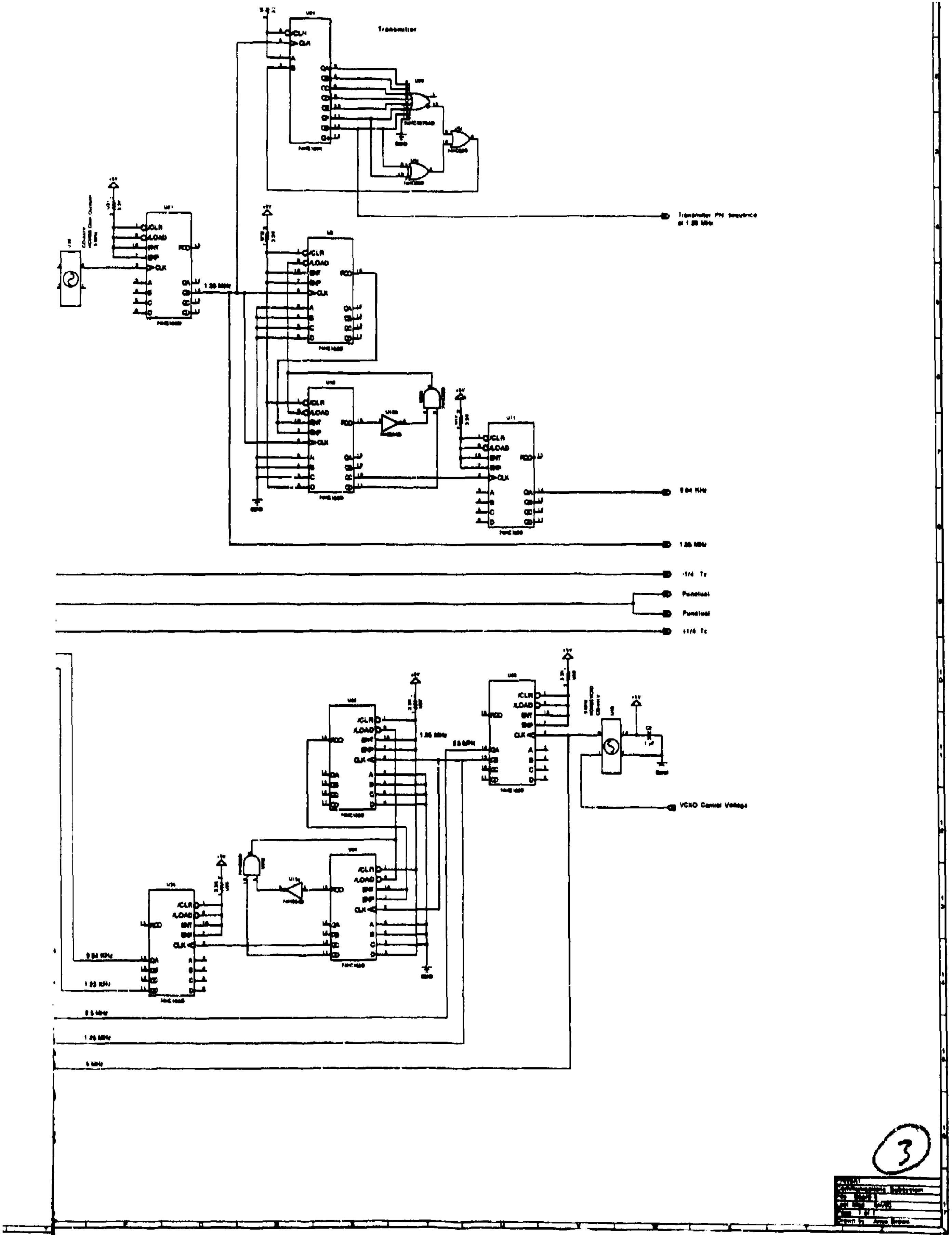

10.7 MHz sinewave from the VCXO approx +7 dBm
J4
SMA
To the Costas Loop in the Demodulator Board 4, J3
10.7 MHz sinewave 90 deg out of phase from the VCXO approx +7 dBm
J5
To the Costas Loop in the Demodulator Board 4, J4
AGND
+15V
-15V
1 uF
Gain = 5
R23
124
R33
499
To the Demodulator Board 4, J2
J6
U17
PM-101
TO-8
Bi-Phase Modulator
-7 dbm
HA-5020
21.4 MHz bi-phase modulated with the punctual PN sequence Approx +7 dBm
Late PN sequence to the Tracking ckt Board 3, J3
J7
21.4 MHz bi-phase modulated with a +1/2Tc PN sequence. Approx +7 dBm
Early PN sequence to the Tracking ckt Board 3, J2
J8
21.4 MHz bi-phase modulated with a -1/2Tc PN sequence. Approx +7 dBm
To the Detector Board 2, J4
J9
21.4 MHz bi-phase modulated with an estimate of the punctual PN sequence. Approx +7 dBm
Gain = 6.5
Transmitter IF going to the Front End Board 1, J4
J10
32.1 MHz sinewave approx +7 dBm
-6.1 dBm
Mixer
To the Fast Acquisition Detector
J11
10.7 MHz sinewave approx +7 dBm
Future use
J12
10.7 MHz sinewave 90 deg out of phase approx +7 dBm
+10.4 dBm
Power Splitter w/50
PANSAT
Communications Subsystem
File Board 5
Last Mod 9/30/93
Page 1 of 1
Drawn by Arnie



1


Transmitter
Transmitter Ph at 1.25 MHz
9.84 MHz
1.25 MHz
-1/4 Td
Punctual
Punctual
+1/4 T-
VCXO Control 1
/CLR
/LOAD
ENT
ENP
CLK
RCO
5 MHz

2


Transmitter
Punctual
Punctual
VCXO Control Voltage
3

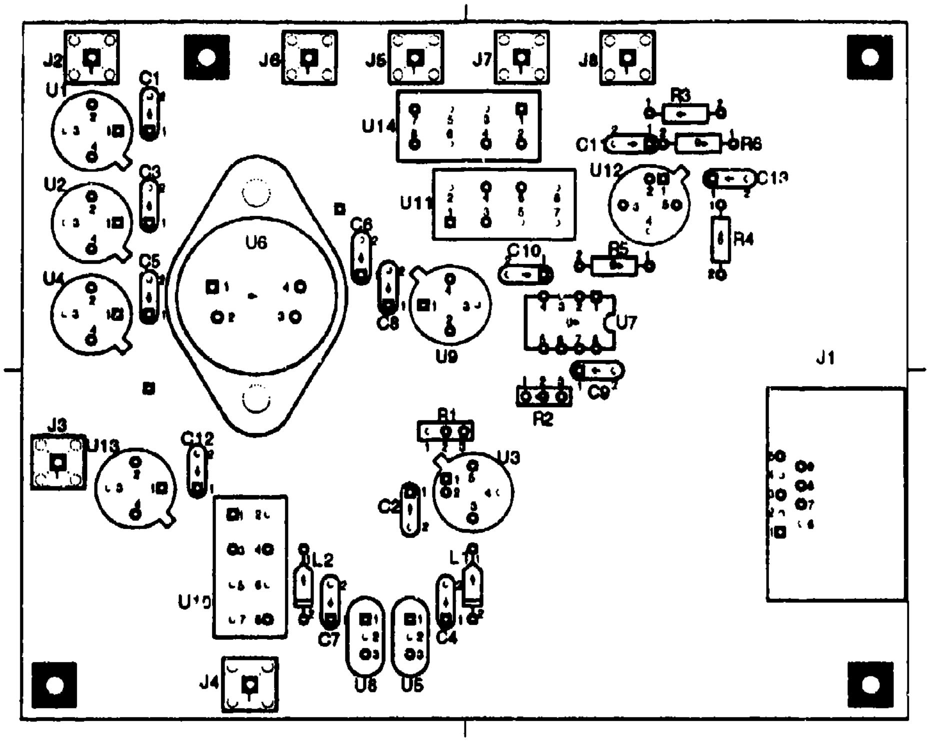


Figure D-14 Layout diagram for Board 2 the Rx IF Amplification, AGC, and Detection circuits.

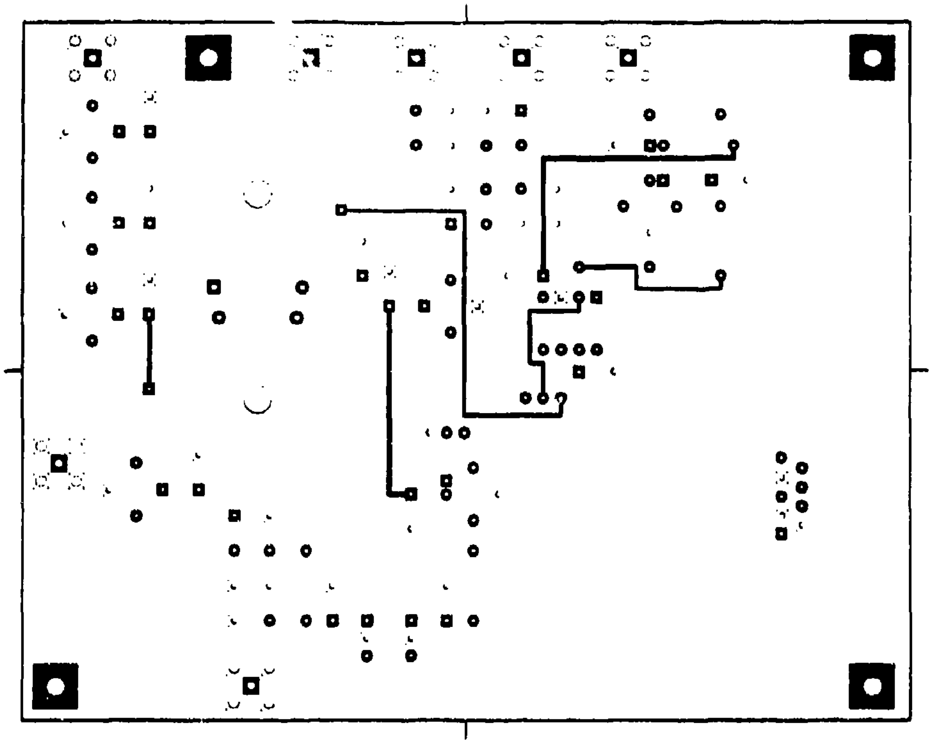


Figure D-15 Component side of Board 2.

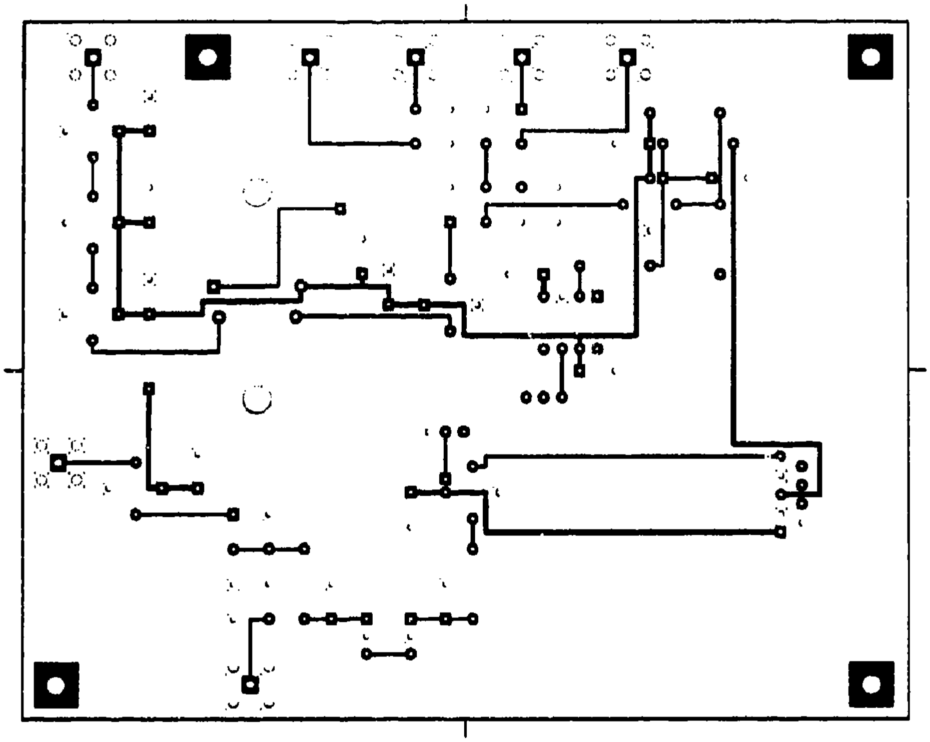


Figure D-16 Solder side of Board 2.

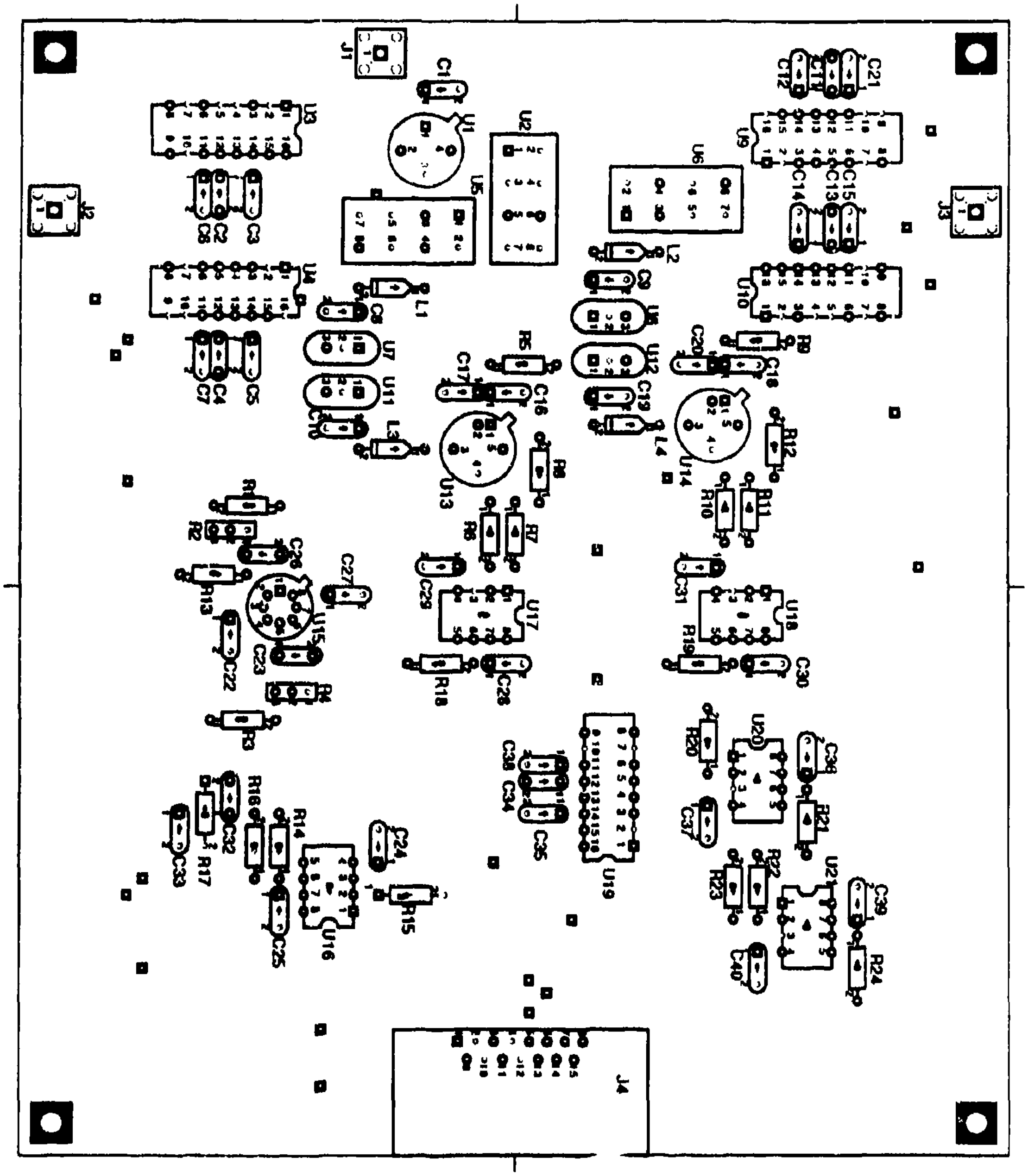


Figure D-17 Layout diagram for Board 3 the PN Sequence and Tracking circuits.

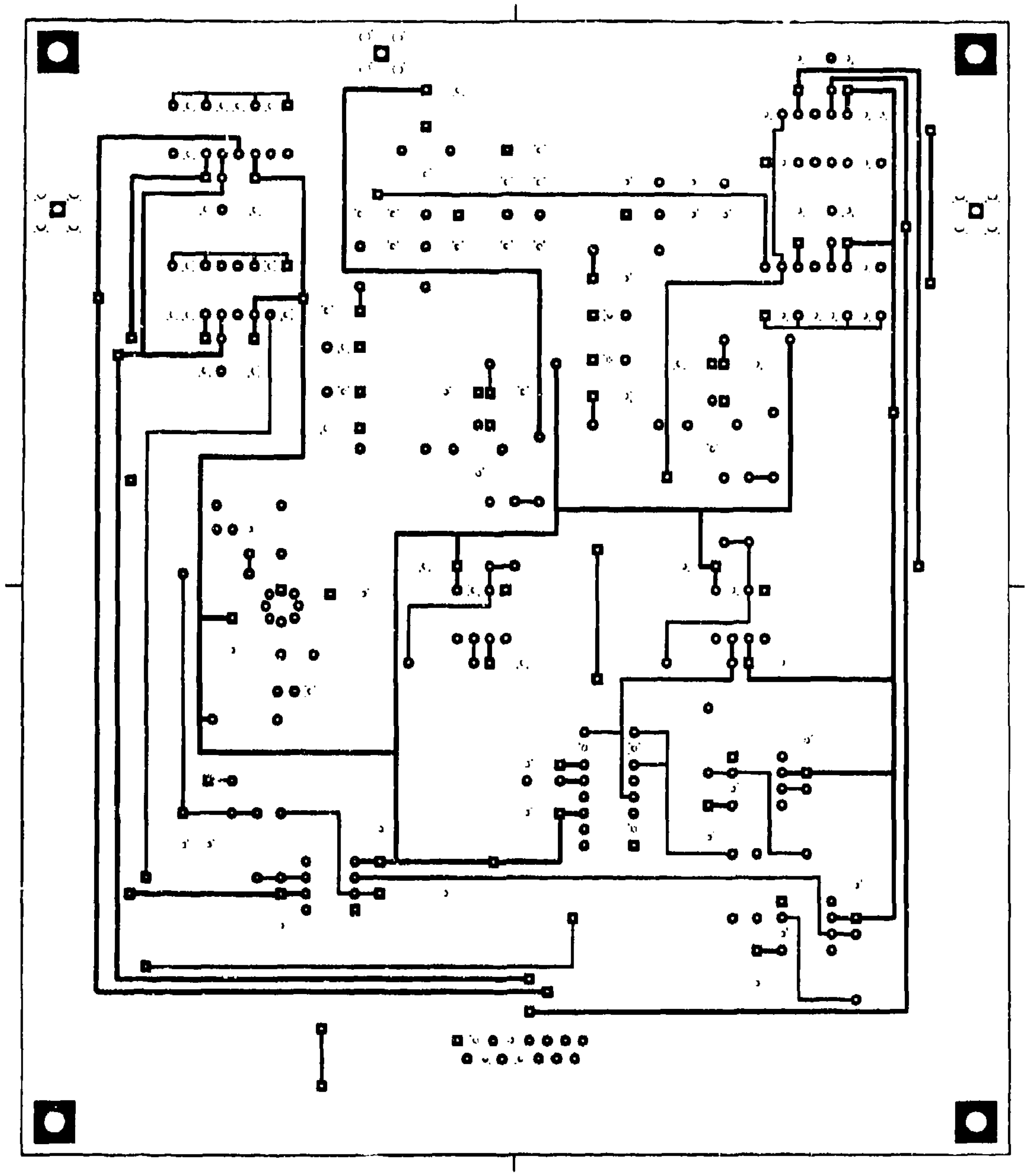


Figure D-18 Component side of Board 3.

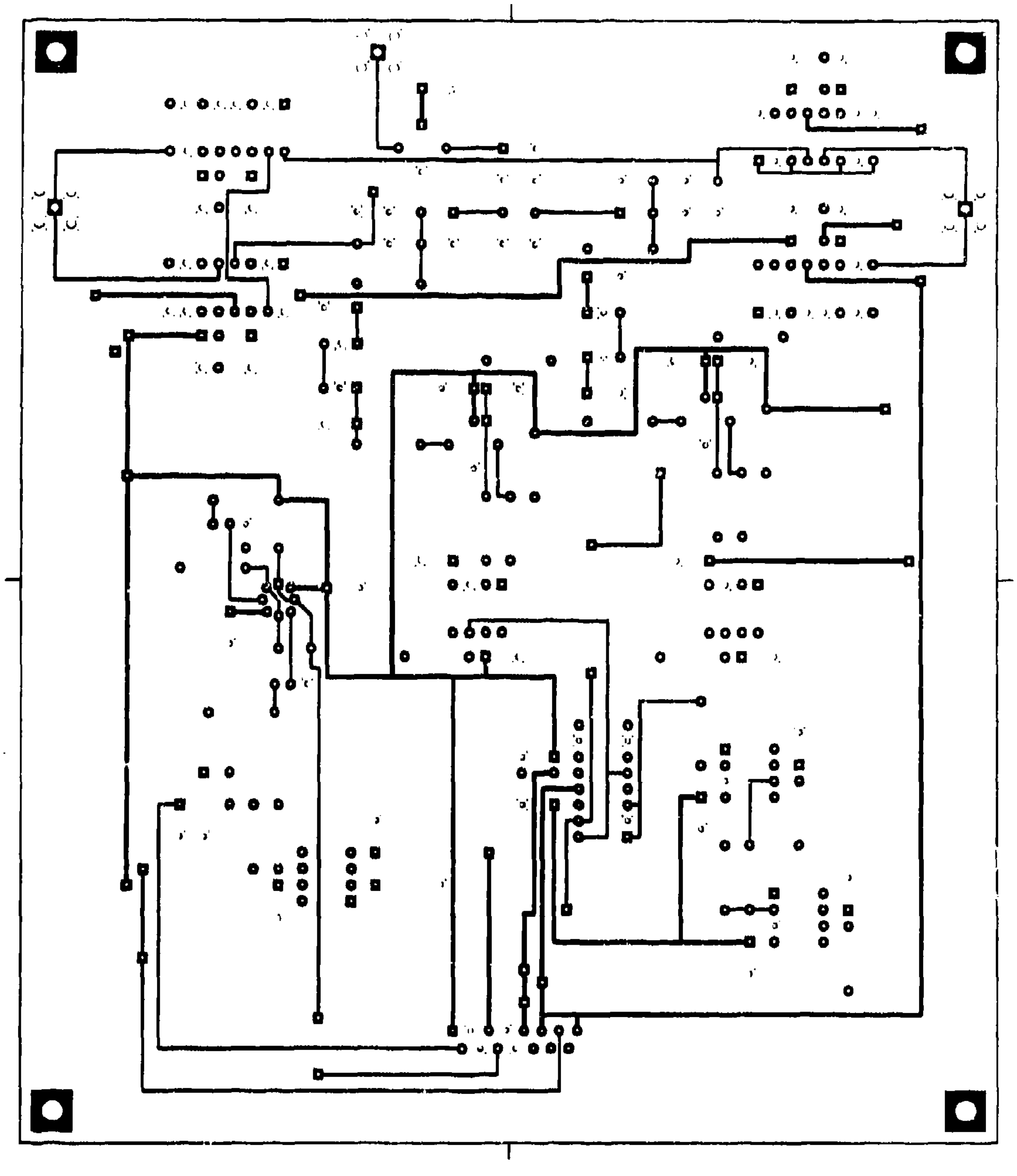


Figure D-19 Solder side of Board 3.

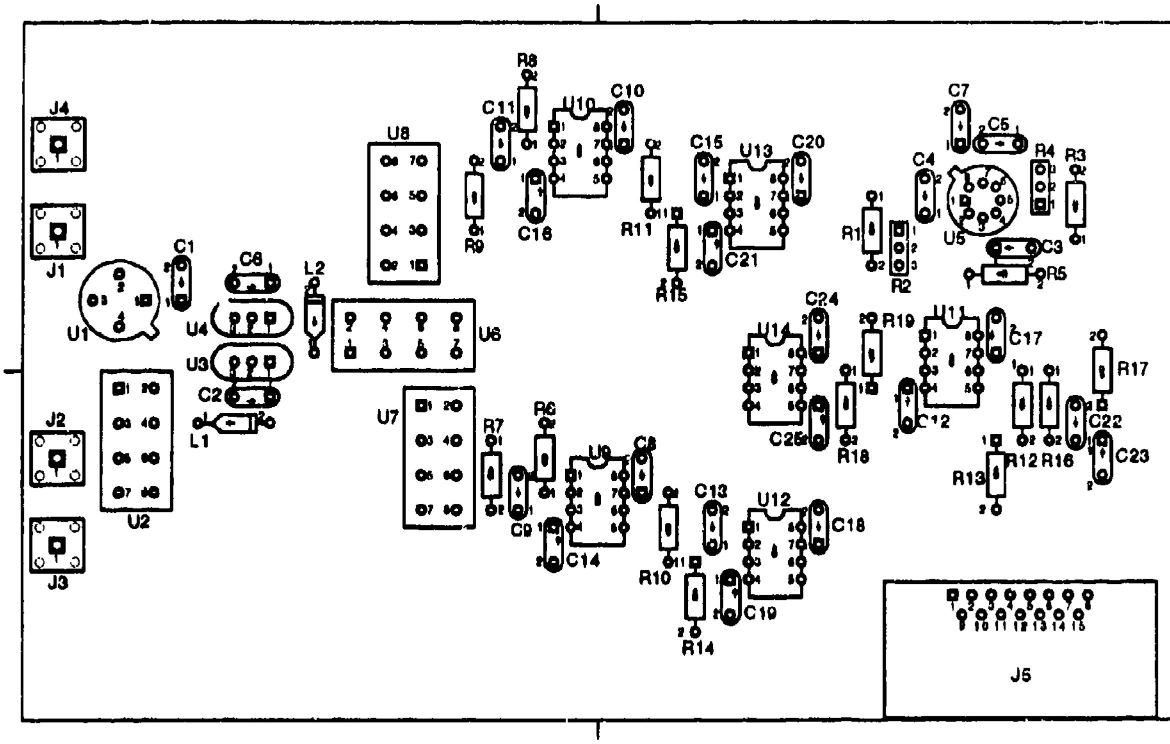


Figure D-20 Layout diagram for Board 4 the Carrier Tracking Loop and Demodulator circuits.

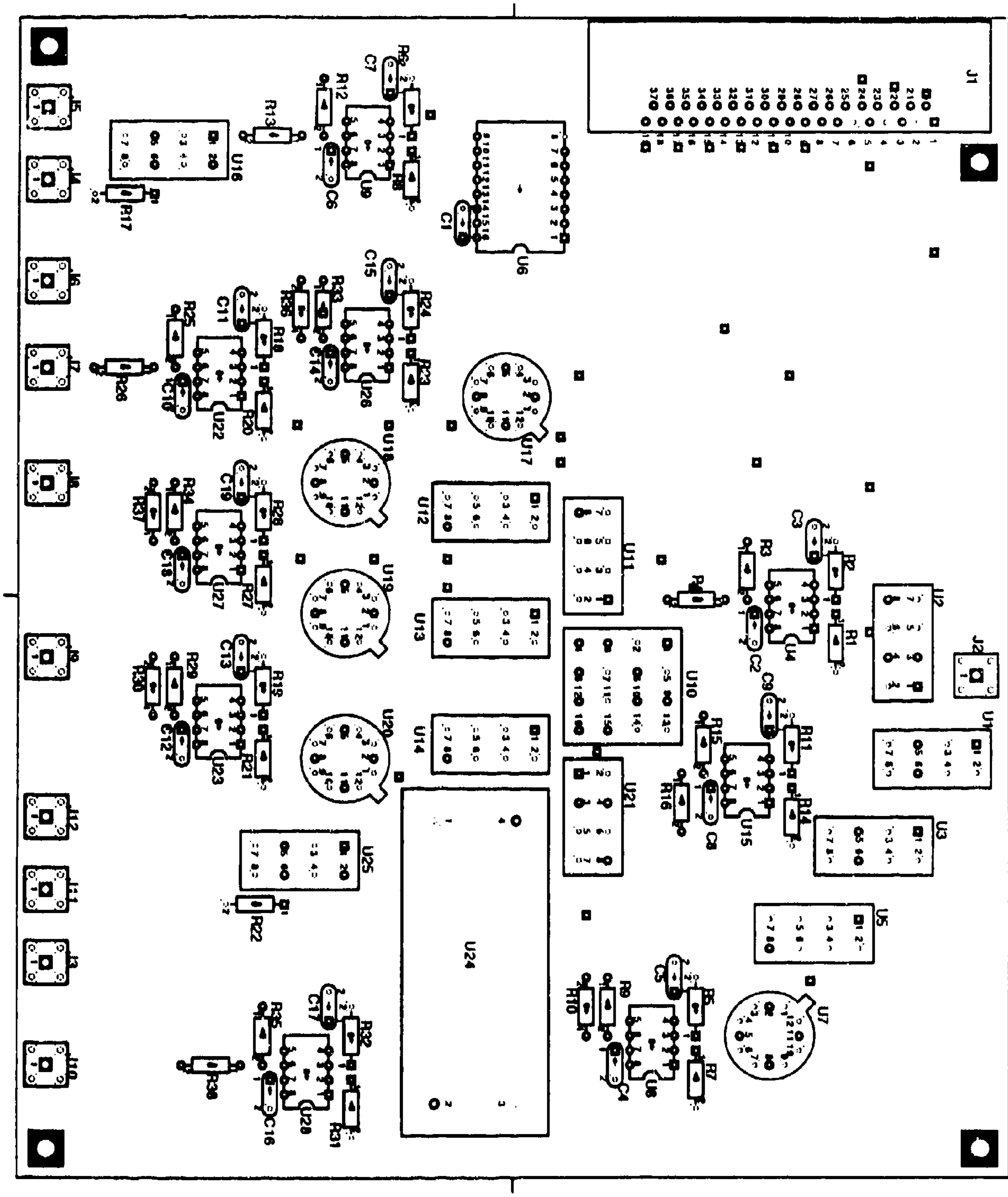


Figure D-21 Layout diagram for Board 5 the Modulation and Amplification circuits.

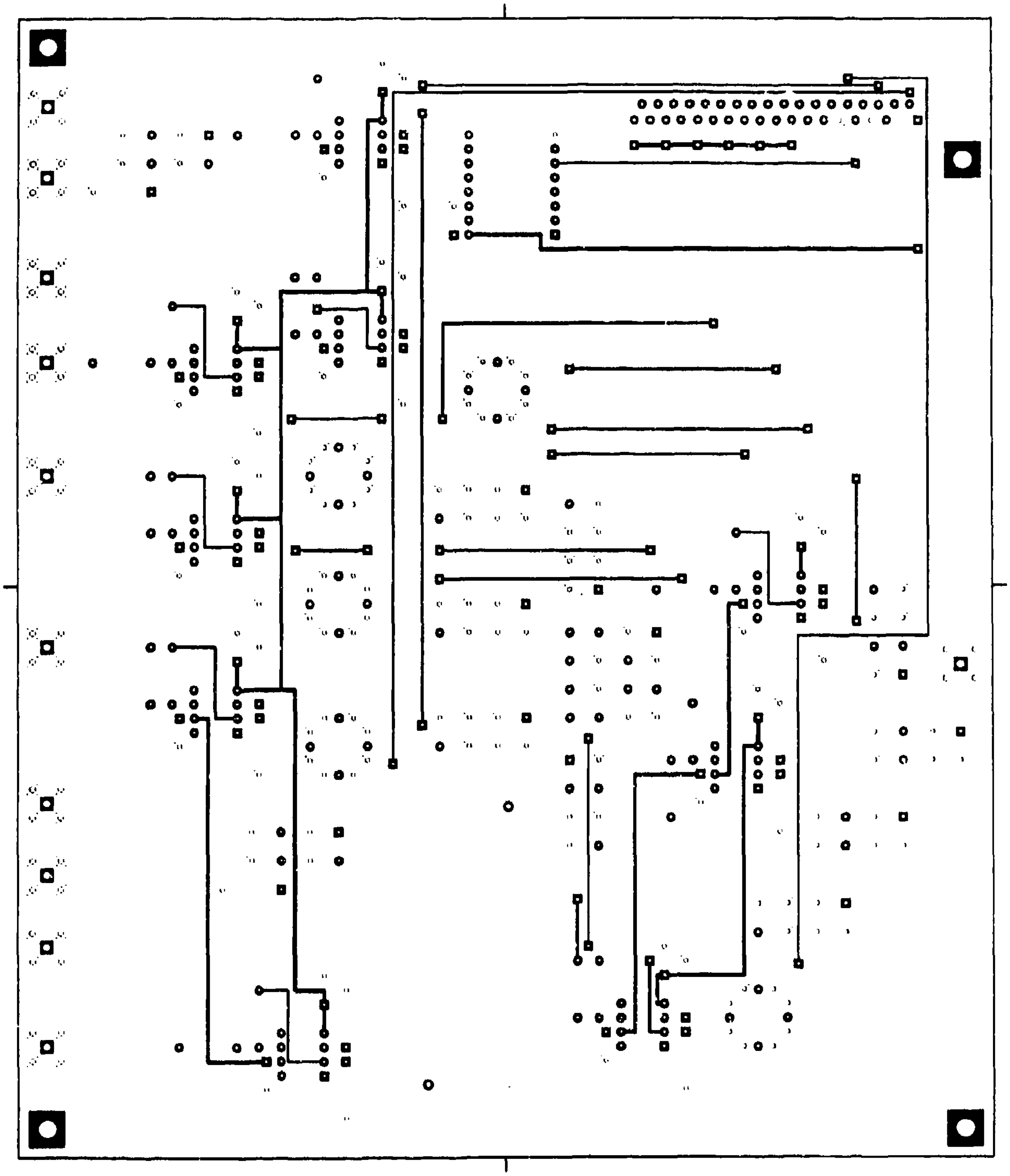


Figure D-22 Component side of Board 5.

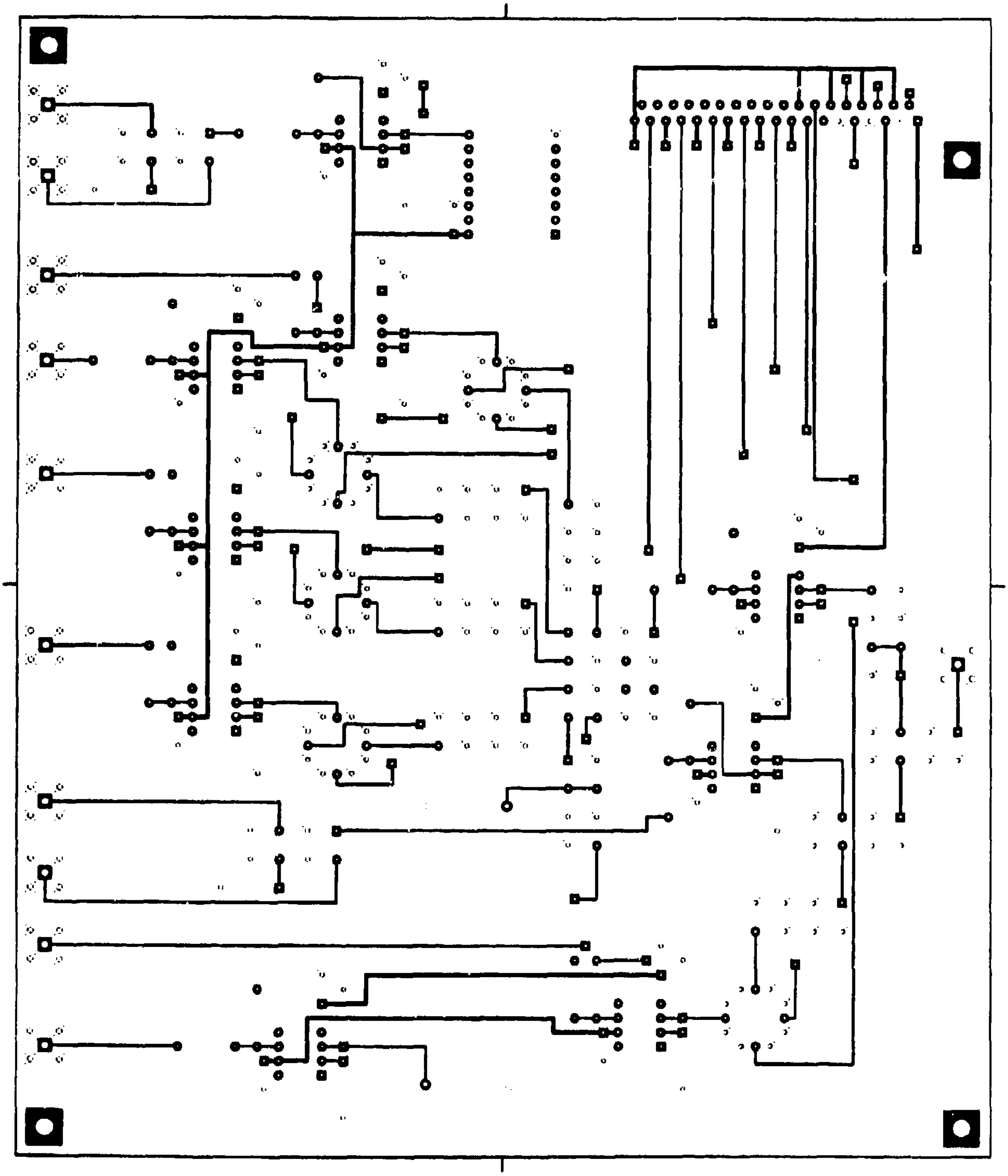


Figure D-23 Solder side of Board 5.

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